WDP FOR 5620AAA101 DOT MAPPED DISPLAY TERMINAL

WDP 0632

DRAWING NO.	SHEET NO.	DESCRIPTION	ISSUE NUMBER																												
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
WDP 0618	ALL	WDP FOR 56D502AAA DOT MAPPED DISPLAY MODULE	1																													
WDP 0607	ALL	WDP FOR M56 KEYBOARDS (56K224 & 56K229)	1																													

TELETYPE CORPORATION

28057R   NOTE : THE LAST COMPLETED COLUMN INDICATES THE LATEST ISSUE NUMBER OF WDP.

SHEET 1 OF 1

R & D FORM 361-0666

WDP 0618

DRAWING NO.	SHEET NO.	DESCRIPTION	ISSUE NUMBER																												
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
		SCHEMATIC WIRING DIAGRAMS																															
4972SD	ALL	TERMINAL LOGIC CARD	1	1	1	2	3	4	4	4																						
4973SD	ALL	I/O FILTER CARD	1	2	2	2	2	2	2	3																						
4862SD	ALL	32B CPU CARD	−	−	−	1	1	1	1	1																						
		CIRCUIT DESCRIPTIONS																															
4972CD	ALL	TERMINAL LOGIC CARD	1	1	1	1	1	2	2	2																						
4862CD	ALL	32B CPU CARD	−	−	−	1	1	1	1	1																						
		ASSEMBLY DRAWINGS																															
410972	ALL	TERMINAL LOGIC CARD	1	4	5	6	7	7	8	9																						
410973	ALL	I/O FILTER CARD	1	2	2	2	2	2	2	3																						
410128	ALL	TERMINAL LOGIC CARD	−	−	−	1	1	2	3	4																						
410862	ALL	32B CPU CARD	−	−	−	1	1	1	1	1																						
		ACTUAL WIRING DIAGRAMS																															
9671WD	ALL	56D502 DISPLAY MODULE	1	2	2	3	3	3	3	3																						
		MARKINGS CHART																															
56D502/MC	ALL	MODEL 56D502 DISPLAY MODULE	1	1	1	2	2	3	3	5																						

TELETYPE CORPORATION

COA 28110   NOTE : THE LAST COMPLETED COLUMN INDICATES THE LATEST ISSUE NUMBER OF WDP.

SHEET 1 OF 1

R & D FORM 361-0666

SHEET INDEX AND ISSUE CONTROL — 4972CD

CIRCUIT DESCRIPTION FOR THE 410972
TERMINAL LOGIC CIRCUIT CARD

Sheet 1 of 3

REVISIONS			SHEET NUMBER																				
ISSUE	DATE	AUTH. NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1	1/17/84	28187R	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	11/14/84	28398	2	1	1	1	1	1	1	1	2	1	1	1	1	1	1	1	1	1	1	1

SHEET ISSUE NUMBER

APPROVALS			ENG. SD	DSGNR.	DRN.	TELETYPE CORPORATION
PROJ. SUPV.	PROJ. DIR.	MFG.REL. COMPL.	DATE	S-NUMBER 62,709S		
			R&D FILE NO. 3-A185.234A	E-NUMBER		4972CD

TC482-0579

SHEET INDEX AND ISSUE CONTROL — 4972CD

CIRCUIT DESCRIPTION FOR THE 410972
TERMINAL LOGIC CIRCUIT CARD.

Sheet 2 of 3

REVISIONS			SHEET NUMBER																		
ISSUE	DATE	AUTH. NO.	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
1	1/17/84	28187R	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	11/14/84	28398	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

SHEET ISSUE NUMBER

APPROVALS			ENG. SD	DSGNR.	DRN.	TELETYPE CORPORATION
PROJ. SUPV.	PROJ. DIR.	MFG.REL. COMPL.	DATE	S-NUMBER 62,709S		
~	~	~	R&D FILE NO. 3-A185.234A	E-NUMBER		4972CD

TC482-0579

CIRCUIT DESCRIPTION FOR THE 410972

TERMINAL LOGIC CIRCUIT CARD

Sheet 3 of 3

REVISIONS

ISSUE	DATE	AUTH. NO.
1	1/17/84	28187R
2	11/14/84	28398

SHEET NUMBER

41	42	43	44	45	46	47	48	49	50
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	2	1	1

SHEET ISSUE NUMBER

APPROVALS

PROJ. SUPV.	PROJ. DIR.	MFG.REL. COMPL.

ENG. SD

DSGNR.

DRN.

DATE

S-NUMBER 62,709S

R&D FILE NO. 3-A185.234A

E-NUMBER

TELETYPE CORPORATION

4972CD

TC482-0579

Section I

CIRCUIT DESCRIPTION FOR THE 410972
TERMINAL LOGIC CIRCUIT CARD

OPERATION AND DESCRIPTION OF THE CIRCUIT

1. **INTRODUCTION**

1.1

The Terminal Logic Circuit (TLC) card (410972) may contain either a WE 32001/BELLMAC 32A (TPN 404132) processor or a WE 32100/BELLMAC 32B CPU Card Assembly (TPN 410862) as the terminal CPU. For those TLC cards equipped with the 32B CPU Card Assembly, disregard SECTION 2 of this document (with the exception of sections 2.11.1-2.11.2 and 2.11.5-2.11.7 which are relevant to both CPUs) and refer in it's place to the 4862 Circuit Description (4862CD). The CPU communicates with the peripheral devices such as Dual Asynchronous Receive/Transmit (DUART), Mouse XY Coordinate Counters (MOUSEXY), and Parallel Input/Output (PIO) circuits. The CPU reads and writes Dynamic Random Access Memory (DRAM), Battery Back-Up Random Access Memory (BBRAM), and Electrically Programmable Read Only Memory (EPROM). Programs executed by the CPU are stored in the EPROM (firmware) and the DRAM. DRAM programs are downloaded from the host computer over the EIA RS232C communications line. The CPU address space selects both peripheral addresses and memory addresses, so there is no distinction between peripheral and memory operations. The peripheral device circuits generate interrupts to the CPU when service is required.

1.2

The TLC card contains video logic that reads the DRAM and converts the bits into dots for the display, and generates horizontal and vertical synchronization signals to control the display monitor.

1.3

The TLC card has three connectors. A video connector links the card to the display monitor and supplies horizontal, vertical, and video signals. A power supply connector links the card to the +12, -12 and +5 volt power supply. An input/output connector links the DUART, MOUSEXY, and PIO peripherals to the 410973 I/O Filter Card.

1.4

Voltage levels for logic signals are:

Voltage	Voltage Range
Low	0.0 to 0.4V
High	2.4 to 5.5V

1.5

This document is constructed as follows: Level one heading titles correspond directly to individual blocks of the 4972SD Block Diagram (except for the section on the Address Space of the TLC Card). After giving a description of each block of the circuit a description of the corresponding Functional Schematics will be given. The notation used in this document is as follows:

- A zero or a one appended to a module function symbol identifies if the signal is active low (0) or active high (1). For example, the physical-address strobe PAS0 is active low, while physical address PAD1 is active high.

- If a signal has two functions, the 0 to 1 suffix is embedded in the symbol name. For example, the function R1W0 identifies a read operation when the signal is high and a write when it is low.

- In some cases, several signals as a group form a single function. For such functions, we always cite the highest and lowest signals (or bits) in the range. For example, consider the signals MA221-MA001 that form the address bus. The rightmost digit identifies the function as active high, while other digits correspond to the bit numbers of the bus. Therefore, MA221 is bit 22 of the address bus and MA001 is bit 0. (Bit numbering always starts at 0.)

- Labeling convention for Logic Devices is as follows:

     ML   H6   -9

  Micrologic   Pin Number Designation

          Board Location
          Row-Col

2. **FS-1 - BELLMAC 32A PROCESSOR**

The BELLMAC 32A processor (CPU) fits naturally into the friendly software environment defined by the UNIX (UNIX is a trademark of Bell Laboratories) system and the C language. The CPU consists of five Very Large-Scale Integrated (VLSI) circuit devices mounted in a single 214 pin epoxy-glass package that measures 3.650 inches long, 2.190 inches wide, and 0.243 inches high. The module operates at 7.2 MHz with +5 Vdc of input power and dissipates about 4 Watts.

2.1 ARCHITECTURAL CHARACTERISTICS

Some of the architectural characteristics of the CPU are:

- Sixteen 32-bit registers for processor and programmer use

- An address arithmetic unit (AAU) that computes addresses and extracts data from the instruction

- A 33-bit ALU that performs arithmetic and logical operations

- A 32-bit barrel switch that performs shift, rotate, and mask operations

- A macro ROM for executing operating system instructions and microsequences

- A 12-byte instruction queue for storing prefetched bytes from the instruction stream.

2.2 INSTRUCTION SET

2.2.1 The module supports a powerful instruction set that includes the standard data transfer, arithmetic, and logical operations for microprocessors, plus several unique operations. Its many program control instructions (branch, jump, return) provide flexibility for altering the sequence in which instructions are executed. Operating system instructions establish an environment that permits other processes to take control of the module.

2.2.2 The processor's instructions are essentially mnemonic-based assembly language statements. Besides defining the operation to be performed, most of the module's instructions also define one of the data types (byte, half-word, or word). Other instructions operate on bit fields (sequences of from one to 32 bits that are contained in a word), or on blocks or strings of data locations.

2.3 MODULE READ AND WRITE

2.3.1 Address and data are transferred within the processor in two stages. In a read or write operation, the module outputs the address during the first two CPU machine cycles of the access and uses the remaining machine cycles for data.

2.3.2 The CPU requires a minimum of two machine cycles for data access. Thus, a read or write operation with cache (fast memory) requires at least four machine cycles. The same operation without cache requires at least five machine cycles. The number of cycles available may be extended with a wait.

2.3.3 The module begins an access by driving address and status onto the corresponding module busses. After address and status have stabilized, the module asserts its address-and-status strobes (active low). The module then checks its fault input (active low) for an address fault.

2.4 FAULTS

2.4.1 Trying to write EPROM and wait timeout are CPU recognized faults. They are reported by an active fault input and terminate bus operation.

2.5 I/O INTERRUPTS

2.5.1 The CPU is connected to two levels of I/O interrupts. Interrupt requests are acknowledged in an interrupt-acknowledge cycle that has the same timing as a read operation. The priority level of the interrupt being acknowledged is inverted and output on bits 2 through 5 of the address bus, and the interrupt vector is read into the module on bits 0 through 7 of the data bus.

2.5.2 After acknowledging the interrupt, the module completes its interrupt sequence which saves the context (internal pointers and registers) of the CPU for the current process. Then, control of the module passes to the operating system's interrupt handler.

2.6 RESET

2.6.1 The module handles two types of reset requests: system and internal. A reset has the highest priority and will interrupt any on-going bus operation.

2.7 EXCEPTIONAL CONDITIONS

2.7.1 In addition to I/O interrupts and reset requests, several types of events may interrupt the execution of a program. The events, called exceptional conditions, may be detected internally by the processor, such as a trap or illegal opcode, or may be generated externally by the hardware such as a memory fault (also see FAULTS). When an exception occurs, the CPU saves the context of the current process and gives the operating system information it needs to locate the correct exception handler. The saved context enables the program to resume executing after the exception is handled.

2.8 DATA HANDLING

2.8.1 Internally, all operations are performed on 32-bit quantities, but data may be read or written as a byte, half-word, or word. Bits are numbered from right to left, starting at 0, and are right adjusted on the bus (both the data bus and the internal microbus). The CPU automatically extends a byte or half-word to 32 bits before performing an operation. Zeros fill the high-order bits for unsigned operations, while the sign bit (bit 7 for bytes, bit 15 for half-words) fills the high-order bits for signed operations.

2.9 DATA IN MEMORY

2.9.1 External memory consists of a series of 8-bit locations for storing data. Half-words occupy two consecutive memory locations; words occupy four consecutive memory locations. Although boundary restrictions apply to the starting location of half-words and words, the module does not generate a fault if these boundaries are violated.

2.10 PIN ASSIGNMENTS

2.10.1 Table I-1 identifies the symbol, pin(s), type, and function assigned to each pin of the BELLMAC 32A processor used by the TLC card. The type may be voltage level, input (I), output (O), or bidirectional input and output (I/O). Pins 001 through 072 are voltages. Of these signals, pins 004, 008, 012, 020, 024, 028, 032, 036, 040, 044, 048, 052, 056, 060, 064, 068, and 072 supply +5 Vdc power to the module, while the other 62 pins serve as module grounds.

TABLE I-1 MODULE SIGNALS BY FUNCTIONAL GROUPS

ADDRESS AND DATA			
NAME	PIN(S)	TYPE	FUNCTION
MA[02-22]1	127, 230, 131, 222, 234, 135, 151, 250, 147, 246, 238, 139, 242, 143, 129, 232, 133, 236, 228, 125, 224	O	Module Address Bus. These pins are the physical address outputs. Outputs are valid when ASO is active. Bits MA[02-06] are also used to output the interrupt acknowledge level during an interrupt acknowledge operation. MA00 is the least significant data bit.
MD[00-311	225, 122, 126, 229, 130, 221, 233, 134, 152, 251, 148, 247, 239, 140, 243, 144, 128, 231, 132, 235, 227, 124, 223, 120, 138, 241, 253, 142, 245, 146, 249, 150	I/O	Module Data Bus. These pins provide a bi-directional bus to transmit data and interrupt vectors to and from the module. MD00 is the least significant data bit.

INTERRUPT SIGNALS			
NAME	PIN(S)	TYPE	FUNCTION
IACKO	210	O	Interrupt Acknowledge. Indicates that an interrupt vector fetch is being performed. The interrupt vector is always a byte 3 (bits 07-00) fetch.
XIPL[0-3]0	204, 207, 206, 205	I	Interrupt Priority Level. These asynchronous inputs indicate the level of the highest priority pending interrupt. Level zero (XIPL[0-3]0 = 1111) indicates no pending interrupts.

RESET SIGNALS			
NAME	PIN(S)	TYPE	FUNCTION
RESETRO	264	I	Reset Request. An asynchronous input to reset the module sampled twice per machine cycle. It must be detected active for two consecutive samplings before being accepted and executed.

TABLE I-1   MODULE SIGNALS BY FUNCTIONAL GROUPS (continued)

INTERFACE CONTROL			
NAME	PIN(S)	TYPE	FUNCTION
ASO	166	O	Address and Status Strobe. Indicates a valid address on the module address bus and valid module bus status on the status bus. Module bus status includes R1WO and IACKO.
CAHITO	259	I	Cache Hit. Indicates that the cache has a hit for the address of the read/write access. It is a synchronous signal and is valid at a pre-determined time with respect to ASO.
DSO	169	O	Composite Data Strobe. This output is the logical OR of the four Byte Data Strobes.
FLTO	267	I	FAULT. Notifies the module of an address or data cycle fault condition. It is treated as an asynchronous input for all address cycle faults and as a synchronous input for data cycle faults.
WS[0-3]O	101, 157, 156, 155	O	Byte Write Strobes. Indicates data is valid on that byte of the module data bus during a write operation. WS00 represents byte 0 (bits 31-24) WS10 represents byte 1 (bits 23-16), WS20 represents byte 2 (bits 15-08), and WS30 represents byte 3 (bits 07-00).
WSEL00	268	I	Wait Selects. This input selects the minimum wait period to be inserted before completing the data cycle. NOTE: This is normally an asynchronous input. Under appropriate timing conditions, however, the Wait Select will produce a synchronous wait period.

CLOCKS			
NAME	PIN(S)	TYPE	FUNCTION
OSCIN1	212	I	Oscillator In. Provides the module clock source. The basic CPU cycle rate is 1/4 of this oscillator frequency.

TABLE I-1   MODULE SIGNALS BY FUNCTIONAL GROUPS (continued)

TEST SIGNALS			
NAME	PIN(S)	TYPE	FUNCTION
TESTO	263	I	Test. Causes all the above module outputs except the system clocks to go into a high impedance state.

2.11 FS-1 DESCRIPTION

2.11.1 Interrupt Logic

2.11.1.1 MLD11-6 Highest level interrupt used on card. Three interrupt sources from:

1. EIA RS232C send buffer ready for data (INT232R).

2. EIA RS232C receive data available (INT232S).

3. PIO interrupt (PIO00).

2.11.2 MLD11-8 Lowest level interrupt used on card. Three interrupt sources from:

1. Keyboard receive data available (INTKBD).

2. Mouse buttons have changed, vertical blank (60 Hz) has started, or EIA RS232C (INTMO).

3. CTS, DSR, DCD lines have changed

4. PIO interrupt (PIO01)

2.11.2.1 MLD12-3, 5, 7, 9, 12, 14, 16, 18 Interrupt Vectors

These six interrupt sources cause 64 interrupt vectors to be generated. The interrupt vectors point to a prioritized transfer vector table that points to the following six interrupt routines.

PIN	ROUTINE
3	Always 0
5	Always 0
7	0 = EIA RS232C receive routine.
9	0 = EIA RS232C send routine.
12	0 = PIO highest level routine.
14	0 = Keyboard routine.
16	0 = Mouse routine.
18	0 = PIO lowest level routine.

2.11.3 Processor Clock

2.11.3.1 MLB13-8 28.8 MHz clock for the processor. The processor generates 14.4 MHz and 7.2 MHz clocks used for processor timing.

2.11.4 Processor MLB15

2.11.4.1 MD001 to MD311 Bidirectional data bus connected to all memory and I/O circuits.

2.11.4.2 R1W0 Read, Write output status line.

2.11.4.3 WS00 to WS30 Byte data true for writing signals. Enables write signals to selected bytes of RAM when the processor has the RAM cycle.

2.11.4.4 TEST0 Floats processor outputs for testing bus.

2.11.4.5 MA021 to MA221 Address true signal.

Other processor signals are input from other parts of the circuit and are discussed as part of those circuits. Unused inputs are pulled to +5V.

2.11.5 Address Decoder

2.11.5.1 MLC12-15 EPROM0 Enables the EPROM's, selects the EPROM cycle time as 4 cycles when OS1 – 8, 9 is closed and as 5 cycles when it is open, and generates a fault when a program attempts to write EPROM.

2.11.5.2 MLC12-13 DUART0 Enables the DUART for a 5 cycle access.

2.11.5.3 MLC12-12 PIO0 Enables the PIO for an asynchronous (TIME 0) external I/O access.

2.11.5.4 MLC12-11 MOUSE0 Enables the MOUSE for a 4 cycle read.

2.11.5.5 MLC12-10 ADDCLK0 Enables the scroll address register for a 4 cycle write.

2.11.5.6 MLC12-9 BRAM0 Enables the non-volatile memory for a 5 cycle read or write.

2.11.5.7 MLC12-7 RAM0 Enables the RAM for an asynchronous (ENSEL00) access.

2.11.6 Watch Dog

2.11.6.1 MLE9-15 Generates a fault when an asynchronous device is not ready after a quarter second time-out.

2.11.7 Field Clock

2.11.7.1 MLC2-9 FIELD1 Generates a 30 Hz signal with transition at the start of vertical blank.

3. ADDRESS SPACE

3.1 OVERVIEW

The CPU addresses 8,388,608 (2**23) bytes of memory and I/O logic on the TLC card. A word in memory consists of 32 bits and is divided into 4 bytes. See Figure I-1 for word division.

```
31    24 23    16 15     8 7      0
| BYTE 0 | BYTE 1 | BYTE 2 | BYTE 3 |
```
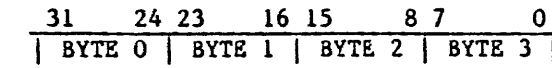
Figure I-1   Word Division

In order to reduce the time required to select a peripheral or memory location, a simple address decoding scheme was used. A single decoder selects one of eight blocks of address space. Each block contains 256K word addresses (1,048,576 byte addresses). The block size is equal to the address space required when 256K DRAM packages are used in the DRAM block. See Figure I-2 for the TLC card Memory Map.

3.2 ADDRESS SPACE ALLOCATION

3.2.1 The first block addresses up to 64K words (000000 to 03FFFF) of EPROM. Addresses 040000 to 0FFFFF are reserved.

3.2.2 The next block, addresses 100000 to 1FFFFF, is not used.

3.2.3 Addresses 200000 to 2FFFFF are devoted to the DUART. The DUART has sixteen internal 8 bit registers, so it uses only sixteen bytes of the block. These registers are mapped onto the address space as shown in Figure I-3. (See also Table I-3). Note that only byte 3 of each word is used. All other unused bytes in the table along with addresses 200040 to 2FFFFF are reserved.

FIGURE I-2

MEMORY MAP

	BYTE 0	BYTE 1	BYTE 2	BYTE 3	
	31 24	23 16	15 8	7 0	
7FFFFC R/W 740000	FUTURE OPTIONAL RAM (NONDISPLAY AREA) 192K x32 BITS				7FFFFF 740003
R/W 700000	BASIC RAM (DISPLAY AREA) 64K x 32 BITS				700003
R/W 600000			BRAM 2K x 8 BITS	601FFF 600002	
WO 500000	DISPLAY START ADDRESS 1 x 16 BITS		500001		
400000	MOUSE 1 x 32 BITS				400003
R/W 300000				PIO 32 x 8 BITS	30007F 300003
R/W 200000				DUART 16 x 8 BITS	20003F 200003
00FFFC RO 008000	EPROM 8K x 32 BITS				0FFFF 008003
RO 000000	EPROM 8K x 32 BITS				000003

FIGURE I-3

Map of DUART Registers onto Address Space

*: Indicates reserved byte location

MEMORY ADDRESS SPACE					DUART ADDRESS
BYTE 0	BYTE 1	BYTE 2	BYTE 3		
*	*	*	200003	<----	0
*	*	*	200007	<----	1
*	*	*	20000B	<----	2
*	*	*	20000F	<----	3
*	*	*	200013	<----	4
*	*	*	200017	<----	5
*	*	*	20001B	<----	6
*	*	*	20001F	<----	7
*	*	*	200023	<----	8
*	*	*	200027	<----	9
*	*	*	20002B	<----	10
*	*	*	20002F	<----	11
*	*	*	200033	<----	12
*	*	*	200037	<----	13
*	*	*	20003B	<----	14
*	*	*	20003F	<----	15

3.2.4 Addresses 300000 to 3FFFFF are devoted to the PIO. The PIO port can be used to address up to thirty-two external 8 bit registers, so it uses only thirty-two bytes of the block. Byte 3 of the first 32 words of the specified space is used. Unused bytes in the first 32 words along with addresses 300080 to 3FFFFF are reserved.

3.2.5 Addresses 400000 to 4FFFFF are set aside for the MOUSEXY. MOUSEXY uses the first word of this space, addresses 400000 to 400003. Addresses 400004 to 4FFFFF are reserved.

3.2.6 Addresses 500000 to 5FFFFF are set aside for the Display Start Address. This 16 bit address is located in byte 0 and byte 1 of the first word of the specified space and can only be written. This start address must be written using only the half-word addressing modes. Memory addresses 500002 to 5FFFFF are reserved.

3.2.7 Addresses 600000 to 6FFFFF are devoted to BBRAM. The 2K bytes needed for the BBRAM are located in byte 2 of the first 2K words of the specified memory space. The first byte occurs at address 600002 and the last byte occurs at 601FFE. All other addresses in this space are reserved.

3.2.8 The next 64k x 32 bits, addresses 700000 to 73FFFF, is devoted to basic DRAM (Display Area). Addresses 740000 to 7FFFFF of DRAM is for future RAM.

4. FS-2, 3, 4, & 5 DYNAMIC RANDOM ACCESS MEMORY (DRAM)

4.1 DESCRIPTION

The TLC card is capable of utilizing either 64K x 32 bits or 256K x 32 bits of DRAM, depending on which of two RAM packages, 64K x 1 bit or 256K x 1 bit, is used. Both modules use a 16 pin package but the 256K pack requires one extra address line to provide access to its additional memory. This extra address line is always wired in but is not used by the 64K x 1 bit package.

4.1.1 Since Dynamic RAM is used, it is necessary to refresh the least significant bits of address every 2msec. This is done when the video circuit reads DRAM to refresh the display.

4.1.2 To read and write DRAM the following control signals, in addition to the data I/O and address lines, are needed:

1. Row Address Select (RAS): On the falling edge of the RAS signal the least significant address levels are loaded into the RAM.

2. Column Address Select (CAS): On the falling edge of the CAS signal the most significant address levels are loaded into RAM. Also, when CAS is low the RAM can be read from or written to.

3. WRITE: When the WRITE signal is low, during CAS low, data can be written and when the WRITE signal is high data can be read.

4.2 FS-2, 3, 4, & 5 DESCRIPTION

4.2.1 Address Multiplexer

4.2.1.1 MLE6, MLF6, MLF7, MLF8, MLF9 Selects the processor or display address and selects the row or column address for the RAM.

4.2.2 Address Drivers

4.2.2.1 MLG7-12, 18 Drive the RAM address bus.

4.2.2.2 MLG8-12, 18 Drive the RAM address bus.

4.2.2.3 MLG6-12, 18 Drive the RAM address bus. (256K RAMS only)

4.2.3 RAM

4.2.3.1 MLL5 to MLL8, MLL10 to MLL13 RAM for 64K x 32 or 256K x 32 bits of memory.

4.2.3.2 MLK5 to MLK8, MLK10 to MLK13 RAM for 64K x 32 or 256K x 32 bits of memory.

4.2.3.3 MLJ5 to MLJ8, MLJ10 to MLJ13 RAM for 64K x 32 or 256K x 32 bits of memory.

4.2.3.4 MLH5 to MLH8, MLH10 to MLH13 RAM for 64K x 32 or 256K x 32 bits of memory.

4.2.4 RAM Data Out Registers for the Processor

4.2.4.1 MLL9, MLK9, MLJ9, MLG9 Hold the processor's RAM data so display servicing can continue.

5. FS-6 MEMORY ARBITER

5.1 OVERVIEW

The DRAM has a arbiter circuit that determines whether the BELLMAC 32A processor or the video circuit has access to memory. The circuit operates on a first come first served basis. If memory is busy the processor or video circuit has to wait for the other to complete its memory cycle. Once memory is given to the processor or video circuit there are five steps to be performed to complete the access cycle. First, the address multiplexers are switched to the processor or video circuit. Next, the RAS signal is generated to load the least significant

bits of the address. The address multiplexers are then switched to the most significant bits of the address and the CAS signal is generated to load these bits. Finally, the read or write operation is performed.

5.2 DETAILED DESCRIPTION

The following description of the Memory Arbiter is based on TABLE I-2. Each numbered entry of this description corresponds directly to the state numbers in TABLE I-2. In the following explanation it shall be assumed that only the processor is requesting RAM for a read or write.

1. Initial condition of the arbiter given that no display or processor requests have been generated for several cycles of the 32MHz clock input at MLA15-10.

2. The Arbiter operation is initiated with a request from the processor, MLE1-13. This low to high transition at MLJ1-4 clocks in a 1 on MLJ1-6 and a 0 on MLJ1-7. This request is then stored in the R-S latch (MLJ2) setting MLJ2-1 to 1. MLJ1-6 causes a zero to occur at MLL3-5. This zero will enable the binary counter (MLL2) on the next positive transition of the 32MHz clock.

   NOTE: All of the following state changes are initiated by every positive edge of the 32MHz clock, excluding state 17.

3. MLL2, binary counter, is enabled. NOTE: The counter's initial state is QA=1, QB=0, QC=0, QD=1.

4. Counter steps to 10.

5. Counter steps to 11. This causes MLL2-9 to be active.

6. The binary counter is loaded with zeros. This activates the RASO signal, MLL2-11. The RASO signal is fed to the binary shift register, which is in the parallel load state, and will be delayed 3 clock cycles and then generate CASO at MLL3-13. WRSTO is activated and ENSELOO is generated for a RAM write request.

7. RASO complemented and delayed one clock cycle generates the SEL1 signal.

8. RASO complemented and delayed 2 clock cycles disables the clear input of the J-K flip-flop (MLJ1-15).

9. CASO is generated.

10. Counter steps to 4.

11. Counter steps to 5.

12. Counter steps to 6.

13. Counter steps to 7.

14. ENSELOO is generated for a RAM read request. RASO is deactivated. This low to high transition of RASO clocks in a 0 on MLJ1-9 which causes MLJ1-7 to go to 1 clearing the R-S latch of the processor request and sets MLL2-5 to 1 which will disable the binary counter on the next clock pulse. PLOAD1 is activated.

15. Counter is disabled and SEL1 is deactivated.

16. CASO is deactivated.

17. Some time later, depending on the BELLMAC timing, PREQ (MLE1-13) will be deactivated.

A display request would generate the same sequence of events as the above except that DQ1 (MLJ2-4) would be 1 and ENSELOO, PLOAD1, and WRSTO would not be generated. If during a processor request a display request is generated, the arbiter will hold the display request until finishing the processor request and then immediately process the display request and vice versa.

TABLE I-2

MEMORY ARBITER CIRCUIT STATE TABLE

STATE		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
MLJ1-4	FREQ	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	
MLJ1-6		0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	
MLJ1-7		1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	
MLJ1-1		1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	
MLJ1-2		1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	
MLJ1-3		1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	
MLJ1-12		1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	
MLJ1-10		0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	
MLJ1-9		1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	
MLJ1-15		0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	
MLJ1-14		0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	
MLJ1-13		0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	
MLJ2-1		0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	
MLJ2-4	DQ1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		1	1
MLJ2-10		1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	
ML13-4		1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	
ML13-5		1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	
ML13-6		1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	
ML13-7		1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	
ML13-15		1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	
ML13-14		1	1		0	0	0	0	0	0	0	0	0	0	0	1	1	1	
ML13-13	CAS	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	
ML13-12		1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	
ML13-11	SEL1	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	
ML12-14		1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	1	1	
ML12-13		0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	0	
ML12-11	RAS	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	
ML12-9		1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	
ML12-10		0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0		
MLF1-3	WESTO	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	
MLJ2-13	ENSEL00	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	READ
MLJ2-13	ENSEL00	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	WRITE

5.3 FS-6 DESCRIPTION

5.3.1 RAM Timing Generator

5.3.1.1 MLA15-10   32 MHz counter clock. The clock is fed through an EXCLUSIVE-OR for purposes of buffering and noise elimination.

5.3.1.2 MLL2-11   RAS signal generated low for counts one through seven.

5.3.1.3 MLL3-11   SEL1 signal switches the RAM address multiplexers from the ROW to the COLUMN address one count after RAS.

5.3.1.4 MLL3-15   Controls the end of the load signal used to clock the RAM data out registers.

5.3.1.5 MLL3-13   CAS signal generated low for counts four through ten.

5.3.2 RAM Data Available For The Display

5.3.2.1 MLK1-7   Loads the RAM data out register for the display and resets the RAM request.

5.3.3 RAM Data Available For The Processor

5.3.3.1 MLJ1-10   Loads the RAM data out register for the processor.

5.3.3.2 MLJ1-9   Resets the processor RAM request.

5.3.4 RAS CAS Drivers

5.3.4.1 MLG6-14, 16   Drive the RAM RAS and CAS bus.

5.3.5 Display RAM Request

5.3.5.1 MLK1-9   Hold the display RAM request until the display has accessed RAM.

5.3.5.2 MLK1-10   Enables counter MLL2 to count from one to eleven thus generating an eleven count memory cycle.

5.3.6 Processor RAM Request

5.3.6.1 MLJ1-7   Holds the processor RAM request until the processor has accessed RAM.

5.3.6.2 MLJ1-6   Enables counter MLL2 to count from one to eleven thus generating an eleven count memory cycle.

5.3.7 RAM Write Delay

5.3.7.1 MLF1-3 Give the processor more time to set up data by delaying the RAM write signal.

5.3.8 RAM Contention Latch

5.3.8.1 MLJ2-1, 4 First come, first served memory cycle latch. A high on MLJ2-1 indicates the processor has the current RAM cycle. A high on MLJ2-4 indicates the display has the current RAM cycle.

5.3.9 RAM Data Out Enable

5.3.9.1 MLK2-2 Enables the RAM data out registers to drive the processor data bus during a processor read cycle.

5.3.10 Processor Request Decode

5.3.10.1 MLE1-13 PREQ1 is the Decoding of the processors RAM request. PREQ1 is active as soon as the address is true for read cycles, so the processor will operate with a minimum read cycle delay. For a write cycle PREQ1 is not active until the write data is true on the processor, so the RAM will not load bad data.

5.3.11 RAM Read Ready For Processor

5.3.11.1 MLH1-6 Prevents the processor from completing a RAM read cycle until the RAM has loaded the processor RAM data out registers.

5.3.12 RAM Write Ready For Processor

5.3.12.1 MLH1-10 Prevents the processor from completing a RAM write cycle until the RAM has granted the processor the current RAM cycle.

5.3.13 RAM Ready For Processor

5.3.13.1 MLJ2-13 A low enables the processor to complete a RAM read or write cycle when the RAM has granted the processors RAM request.

6. FS-7, 8, & 9 - DISPLAY TIMING, VIDEO TIMING, AND SHIFT REGISTERS

6.1 OVERVIEW

The Video circuitry is used to transform bits stored in the DRAM to images displayed on the screen. For proper circuit operation it is necessary to load the sixteen least significant levels of the start address of the first word to be displayed in the Display Start Address register located at 500000H.

The display consists of a matrix of 800 dots by 1024 dots at 100 dots per inch resolution. At the beginning of the display cycle the start address of the first word stored in the Display Start Address register is loaded into the Display Address counter. As the display is scanned from left to right and top to bottom the Display Address counter reads consecutive locations in memory into the video shift register for serializing. The video shift register takes 32 parallel data bits and converts them to a serial video signal. Since there are 32 bits in each word read, 25 words are read each time the video beam traces the screen from left to right. This must be repeated 1024 times to fill the entire screen. In addition, the video circuit also generates horizontal and vertical synchronizing signals. The synchronizing signals control the monitor so the video image is displayed properly.

The video circuit provides an interlaced timing for flicker free operation at a 30Hz refresh rate. As stated above there are 1024 scans of the display. In interlaced operation odd scans are laid down in one pass followed by the even scans in the second pass of the screen. Each individual pass takes 1/60 of a second so the entire screen is refreshed 30 times per second.

6.2 FS-7 DISPLAY TIMING DESCRIPTION

6.2.1 Vertical Scan Counter

6.2.1.1 MLB4, MLB3, MLA2 Modulus 1067 counter counts from 0 to 1066 at 64.02 kHz. Two counts for every horizontal scan. The 1067 horizontal scans are divided into 533.5 for the odd and even fields of the frame. The 533.5 scans per field are divided into 512 for the displayed part of the vertical scan, and 21.5 for the retrace part of the vertical scan.

6.2.2 Horizontal Scan Counter

6.2.2.1 MLA6, MLA5 Modulus 128 counter counts from 0 to 127 using a 4 MHz clock. One count for every eight horizontal dots on the screen. The 1024 dot intervals are divided into 800 for the displayed part of a horizontal scan, and 224 for the retrace part of a horizontal scan.

6.2 3 Vertical Scan Signals

6.2.3.1 MLC5-2 DOG CLK1 60 Hz clock used for the processor watch dog timer and the DUART vertical blank interrupt circuits.

6.2.3.2 MLC5-19 VSYNC Synchronizes the vertical deflection circuit in the display monitor with the video signal. The vertical sweep frequency is 60 Hz.

6.2.3.3 MLC2-6 Generates a vertical blank signal when the vertical scan is returning from the bottom to the top of the screen.

6.2.3.4 <u>MLC3-8</u> Resets the vertical scan counter at count 1066.

6.2.4 <u>Horizontal Scan Signals</u>

6.2.4.1 <u>MLC4-6 ADDCNT</u> Enables the display address counter to increment twenty-five times during the displayed part of the horizontal scan and another twenty-five times during the retrace part of horizontal scan. The resulting twenty-five displayed addresses are used to read 800 RAM bits per horizontal scan into the video shift registers. The twenty-five retrace addresses are not used for this field but will be used on the next field to generate the other half of the scan lines. Note! The display uses interlaced scan, so the odd scans are displayed during the odd field and the even scans are displayed during the even field. An even field and an odd field (a frame) make up a complete image. The complete image must be refreshed 30 times a second.

6.2.4.2 <u>MLC4-7 DREQ1</u> Request twenty-five display RAM read cycles every horizontal scan. The requests are generated as soon as the display RAM data out registers are available. The RAM has 32 dot clock cycles to load the requested data into the display RAM data out registers. If the display request had to wait for a processor request it would take a maximum of twenty-two dot clock cycles to load data.

6.2.4.3 <u>MLC4-8</u> Enable the vertical scan counter to increment twice every horizontal scan. The vertical scan counter increments at the end and middle of each horizontal scan. The odd and even fields are caused to interlace by starting vertical retrace at the end of a horizontal scan for odd fields and at the middle of a horizontal scan for even fields.

6.2.4.4 <u>MLC4-9</u> Resets the horizontal scan counter at count 127.

6.2.4.5 <u>MLC4-11 ADDLOAD</u> Loads the start address register, which contains the address of the first 32 dots displayed, into the display address counter during vertical retrace blank when the display is not reading RAM.

6.2.4.6 <u>MLC5-15</u> Clocks the vertical blank signal on MLC2-6 so the vertical blank starts and ends during horizontal blank. Blank occurs when the horizontal scan is returning from the right to the left side of the screen and when the vertical scan is returning from the bottom to the top of the screen.

6.2.4.7 <u>MLC4-14 HSYNC</u> Synchronizes the horizontal deflection circuit in the display monitor with the video signal. The horizontal sweep frequency is 32.01 kHz.

6.3 <u>FS-8 DISPLAY ADDRESS DESCRIPTION</u>

6.3.1 <u>Display Start Address Registers</u>

6.3.1.1 <u>MLD2, MLD3</u> These chips are loaded by the processor and contain the address of the first word of the first scan line displayed on the screen.

6.3.2 <u>Display Address Counter</u>

6.3.2.1 <u>MLE5, MLE4, MLE3, MLE2</u> These chips are loaded from the display start address registers at the start of each field. The even scan line field uses the start address and the next twenty-four word addresses to read the 800 dots of the first scan (scan line 0). The address counter is then advanced twenty-five addresses during horizontal retrace blanks and the next twenty-five addresses are used for scan line 2. The odd scan line field advances the start address by twenty-five addresses before reading the first word of the second scan line (scan line 1). The entire display refresh cycle consists of: reading and displaying the even field (all the even scan lines from 0 to 1022), followed by reading and displaying the odd field (all the odd scan lines from 1 to 1023).

6.4 <u>FS-9 VIDEO TIMING & SHIFT REGISTERS DESCRIPTION</u>

6.4.1 <u>RAM Data Out Registers for the Display</u>

6.4.1.1 <u>MLG2, MLG3, MLG4, MLG5</u> These chips are loaded by the memory arbiter circuit in response to a request for data from the display timing circuit. They contain the next thirty-two dots to be loaded into the low speed video shift register.

6.4.2 <u>Low Speed Shift Registers</u>

6.4.2.1 <u>MLF2, MLF3, MLF4, MLF5</u> These chips are loaded from the RAM data out registers for the display. They are loaded in parallel with all thirty-two dots when the high speed video Shift Register is shifting the last four dots of the previous thirty-two dots. After loading, the four shift registers that comprise the low speed video shift registers are shifted in parallel causing eight sequences of four dots to be presented to the high speed video shift registers. The low speed video shift registers are not loaded during retrace blank, but do continue to shift out a blank video.

6.4.3 <u>High Speed Video Shift Register</u>

6.4.3.1 <u>MLD13</u> This chip parallel loads the four dots from the low speed video shift registers and serially shifts out the dots at the display clock rate.

6.4.4 <u>Dot Counter</u>

6.4.4.1 <u>MLC12</u> This chip is a counter used to divide the display clock into secondary clocks used in video timing. MLH2-3 loads the high speed, four bit, video shift register by generating one pulse every four display clocks. MLH2-6 increments the horizontal scan line counter every eight displayed dots. MLH3-6 loads the low speed thirty-two bit video shift register by generating one pulse every thirty-two display clocks.

6.4.5 Display Clock

6.4.5.1 **MLA13** This chip generates a 32.77824 MHz dot signal used for video and RAM timing. This frequency is based on a 30 Hz refresh of 1067 scan lines where each scan line consists of thirty-two words and each word of thirty-two bits.

6.4.6 Video Driver

6.4.6.1 **MLD9** This chip drives the video signal to the display monitor.

6.4.7 Reverse Video Gate

6.4.7.1 **MLA15** This chip causes the video to be reversed (inverted) for the entire screen. Retrace blank is also blank for reversed screens because the blank input to the low speed video shift registers is also inverted.

7. FS-10 - MOUSE DECODING

The MOUSEXY circuit is identical for the X and Y coordinates. Each coordinate has a 12 bit up/down counter. Serial signals from the mouse cause the counters to count up when the mouse is moved forward and down when moved backwards. No interrupts are generated by the MOUSEXY circuit and the MOUSEXY counters can only be read. Since no interrupts are generated the program either reads the MOUSEXY in a random fashion under program control or uses the vertical interrupt from the DUART circuit to read the MOUSEXY and update its cursor during video blank.

7.1 FS-10 DESCRIPTION

7.1.1 Y Mouse Counter

7.1.1.1 **MLC9, MKC8, MLC7** These chips are up-down counters that transform the Y movements of the mouse into a Y coordinate used to locate the mouse cursor on the screen. The Y Mouse Counter is identical to the X Mouse Counter in operation. See X Mouse Counter for more information.

7.1.2 X Mouse Counter

7.1.2.1 **MLC6, MKD5, MLD4** These chips are up-down counters that transform the X movements of the mouse into a X coordinate used to locate the mouse cursor on the screen. PAL MLC6 contains circuits that convert the two serial clock signals X0, X1 from the mouse into a count up-down control signal and a clock signal. MLC6 also contains a four bit up-down counter that provides the first four levels of the X coordinate and enables MLD5 to provide the second four levels of the X coordinate. MLD5 enables MLD4 to provide the third four levels of the X coordinate. The mouse handler software reads the counters and converts the 12 bit coordinate into the address of the mouse cursor.

7.1.3 Mouse Button Buffers

7.1.3.1 **MLD6-3,5,7** This chip isolates the MOS DUART from the external mouse buttons and provides input hysteresis to improve noise margins.

8. FS-11 - KEYBOARD AND EIA INTERFACES

8.1 DESCRIPTION OF THE DUAL ASYNCHRONOUS RECEIVE/TRANSMIT (DUART)

The 404381 DUART provides two independent asynchronous receiver/transmitter channels in a single package. The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates. The baud rate generator operates directly from a crystal. Each receiver is buffered to minimize the potential receiver overrun and to reduce interrupt overhead in interrupt driven systems.

8.1.1 The DUART, besides having 2 asynchronous serial send receive ports, also interfaces the processor to individual I/O signals on the circuit board.

8.1.2 Input 0, Input 1, and Input 3 (MB2, MB1, and MB0 respectively) are connected to the 3 buttons on the MOUSEXY. Whenever a button is depressed or released the DUART will send an interrupt to the processor if it is programmed to do so. In normal operation, depression and release of the MOUSEXY buttons causes data to be selected or moved.

8.1.3 Input 2 (DOG CLK) is a signal from the video section that indicates the screen is blanked. This input will generate two interrupts to the processor 60 times per second. Interrupts occur at the start (DOG CLK = 0) and end (DOG CLK = 1) of vertical blank. Programs use this interrupt to update screen images such as the MOUSEXY cursor during blank so flicker does not occur. DOG CLK can also be used as a clock input to a Counter/Timer (C/T) circuit inside the DUART. The C/T circuit can generate time intervals and interrupt the processor at the end of time out.

8.1.4 Input 4, Input 5, and Input 6 (IP4,IP5, and IP6 respectively) are used to receive the following control information via the EIA RS232C line from the host computer.

- IP4: Clear To Send (CTS)

- IP5: Data Set Ready (DSR)

- IP6: Data Carrier Detect (DCD)

8.1.5 Output 0 and Output 7 (OP0 and OP7) are used to control the EIA RS232C link to the host computer. OP0 sends Data Terminal Ready (DTR) to the host and OP7 sends DTR to an auxiliary send only EIA RS232C printer port.

8.1.6 Output 1 (OP1) is used to invert the video signal.

- OP1 = 0: dark background

- OP1 = 1: green background

8.1.7 Output 3 (OP3) is used as the selection control line for multiplexing the send signal to the keyboard (OP3 = 1) or the auxiliary EIA RS232C auxiliary printer port (OP3 = 0). This signal can be used to direct the control words to the keyboard or direct data to the auxiliary printer.

Note: The receive port from the keyboard is used only for the keyboard.

8.1.8 Output 4, Output 5, and Output 6 (INT232R, INTKBD, and INT232S respectively) can be used to interrupt the processor. INT232R interrupts when data is received on the EIA RS232C port. INTKBD interrupts when data is received from the keyboard. INT232S interrupts when the EIA RS232C send register is empty. The EIA RS232C line has dedicated serial I/O ports on the DUART. A general purpose interrupt to the processor is used for other interrupt conditions such as the MOUSEXY buttons.

8.1.9 Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR). The IMR may be programmed to select only certain conditions to cause an interrupt. The ISR can be read by the CPU to determine all currently active interrupting conditions.

8.1.10 The baud rate of all of the EIA RS232C send and receive lines can be programmed to be any commonly used baud rate. The baud rate of the keyboard interface is 4800 baud per keyboard requirements. When the keyboard send line is used for the auxiliary printer, any normal baud rate can be used. The DUART interfaces to the processor by eight parallel bidirectional data signals.

8.2 BAUD RATE GENERATOR

The Baud Rate Generator (BRG) operates from the crystal oscillator (X1) and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. The clock outputs from the BRG are at 16X the actual baud rate. The C/T can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or an external timing signal.

8.3 COMMUNICATIONS CHANNELS

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data. The receiver accepts serial data on the Receive Serial Data (RxD) pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU.

8.4 INPUT PORT

Four change-of-state detectors are provided which are associated with inputs MB0, DOG CLK, MB1, and MB2. A high-to-low or low-to-high transition of these inputs lasting longer than 25-50 micro-seconds will set the corresponding bit in the Input Port Change Register (IPCR). The bits are cleared when the register is read by the CPU. Any change of state can also be programmed to generate an interrupt to the CPU.

8.5 OUTPUT PORT

The 8-bit multi-purpose output port can be used as a general purpose output port, in which case the outputs are the complements of the Output Port Register (OPR). OPR[n]=1 results in OP[n]=low and vice-versa. Bits of the OPR can be individually set and reset. A bit is set by performing a write operation at address 20003B with the accompanying data specifying the bits to be set (1=set, 0=no change). Likewise, a bit is reset by a write at address 20003F with the accompanying data specifying the bits to be reset (1=reset, 0=no change).

8.6 TRANSMITTER

The DUART is conditioned to transmit data when the transmitter is enabled through the Command Register (CR). The DUART indicates to the CPU that it is ready to accept a character by setting the Transmitter Ready (TxRDY) bit in the status register. This condition can be programmed to generate an interrupt request at OP6. When a character is loaded into the Transmit Holding Register (THR), the above conditions are negated. Data is transferred from the THR to the Transmit Shift Register (TSR) when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again which means one full character time of buffering is provided. Characters cannot be loaded into the THR while the transmitter is disabled.

8.6.1 The transmitter converts the parallel data from the CPU to a serial bit stream on the Transmit Serial Data (TxD) output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains high and the Transmitter Empty (TxEMT) bit in the Status Register (SR) will be set to 1. If the transmitter is disabled, it continues operating until the character currently being transmitted is completely sent out. The transmitter can be forced to send a continuous low condition by issuing a send break command.

8.7 RECEIVER

The DUART is conditioned to receive data when enabled through the command register. The receiver looks for a high to low (mark to space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7-1/2 clocks. If the RxD signal is

sampled high, the start bit is invalid and the search for a valid start bit begins again. If the RxD signal is still low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and the parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the Receive Holding Register (RHR) and the Receiver Ready (RxRDY) bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at INT232R and INTKBD for the EIA RS232C input and the keyboard input respectively.

8.7.1 After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point.

8.7.2 The parity error, framing error, overrun error and received break state (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RHR and the received break bit in the SR is set to 1. The RxD input must return to a high condition for at least one-half bit time before a search for the next start bit begins.

8.7.3 The RHR consists of a First-In-First-Out Data Buffer (FIFO) with a capacity of three characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FIFO Full (FFULL) status bit is set if all three stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data in the FIFO and its associated status bits are 'popped' thus emptying a FIFO position for new data.

8.7.4 In addition to the data word, three status bits (Parity Error (PE), Framing Error (FE), and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis: the status applies only to the character at the top of the FIFO. In the characters coming to the top of the FIFO since the last 'reset error' command was issued. The FIFO is 'popped' only when the RHR is read. Therefore the status register should be read prior to reading the FIFO.

8.7.5 If the FIFO is full when a new character is received, that character is held in the receive shift register until an FIFO position is available. If an additional character is received while this state exists, the contents of the FIFO are not affected: the character previously in the shift register is lost and the overrun error status bit (SR[4]) will be set upon receipt of the start

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bit of the new (overrunning) character.

8.7.6 If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No additional characters can be received until the receiver is enabled again.

8.8 PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table I-3.

Table I-3   DUART REGISTER ADDRESSING

ADDRESS	READ	WRITE
200003	Mode Register A(MR1A,MR2A)	Mode Register A(MR1A,MR2A)
200007	Status Register A(SRA)	Clock Select Reg. A(CSRA)
20000B	*Reserved*	Command Register A(CRA)
20000F	RX Holding Register A(RHRA)	TX Holding Reg. A(THRA)
200013	Input Port Chg. Reg.(IPCR)	Aux. Control Reg. (ACR)
200017	Interrupt Status Reg.(ISR)	Interrupt Mask Reg. (IMR)
20001B	Counter/Timer Upper (CTU)	C/T Upper Register (CTUR)
20001F	Counter/Timer Lower (CTL)	C/T Lower Register (CTLR)
200023	Mode Register B(MR1B,MR2B)	Mode Register B(MR1B,MR2B)
200027	Status Register B(SRB)	Clock Select Reg. B(CSRB)
20002B	*Reserved*	Command Register B(CRB)
20002F	RX Holding Reg. B(RHRB)	TX Holding Reg. B(THRB)
200033	*Reserved*	*Reserved*
200037	Input Port	Output Port Conf.Reg.(OPCR)
20003B	Start Counter Command	Set Output Port Bits Command
20003F	Stop Counter Command	Reset Otpt Port Bits Command

8.8.1 The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems. For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the Mode Register (MR), the Clock Select Register CSR, and the Output Port Configuration Register OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the

Auxiliary Control Register ACR should only be made while the C/T is stopped.

8.8.2 Mode Registers 1 and 2 (MR1 and MR2 respectively) of each channel are accessed via independent auxiliary pointers. The pointer is set to MR1A (MR1B) by RESET or by issuing a "reset" command via the corresponding command register CRA (CRB) or at Power On Reset (POR). Any read or write of the mode register while the pointer is at MR1A (MR1B) switches he pointer to MR2A (MR2B). The pointer then remains at MR2A (MR2B), so tha. subseque.t accesses are always to MR2A (MR2B) unless the pointer is reset to MR1A (MR1B) as described above.

8.8.3 Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table I-4a and I-3b for register bit descriptions.

TABLE I-4a DUART REGISTER BIT DESCRIPTIONS

	BIT7	BIT6	BIT5	BIT4 BIT3	BIT2	BIT1 BIT0
	RX RTS CONTROL	RX INT SELECT	ERROR MODE	PARITY MODE	PARITY TYPE	BITS PER CHAR
MR1A MR1B	0=no	0=RXRDY	0=char	00=with parity	0=even	00=5
	1=yes	1=FFULL	1=block	01=force parity	1=odd	01=6
				10=no parity		10=7
	Must be 0			11=not used		11=8

	BIT7 BIT6	BIT5	BIT4	BIT3 BIT2 BIT1 BIT0
	CHANNEL MODE	TxRTS CONTROL	CTS ENABLE Tx	STOP BIT LENGTH*
MR2A MR2B	00=normal	0=no	0=no	0=0.563 4=0.813 8=1.563 C=1.813
	01=Auto echo	1=yes	1=yes	1=0.625 5=0.875 9=1.625 D=1.875
	10=Local loop			2=0.688 6=0.938 A=1.688 E=1.938
	11=Remote loop	Must be 0	Must be 0	3=0.750 7=1.000 B=1.750 F=2.000

*Add 0.5 to values shown for 0-7 if channel is programmed for 5 bits/char.

	BIT7 BIT6 BIT5 BIT4	BIT3 BIT2 BIT1 BIT0
CSRA CSRB	RECEIVER CLOCK SELECT	TRANSMITTER CLOCK SELECT
	see text	see text

	BIT7	BIT6 BIT5 BIT4	BIT3	BIT2	BIT1	BIT0
	not used	MISCELLANEOUS COMMANDS	DISABLE Tx	ENABLE Tx	DISABLE Rx	ENABLE Rx
CRA CRB	must be 0	see text	0=no 1=yes	0=no 1=yes	0=no 1=yes	0=no 1=yes

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	RECEIVED BREAK	FRAMING ERROR	PARITY ERROR	OVERRUN ERROR	TxEMT	TxRDY	FFULL	RxRDY
SRA SRB	0=no 1=yes *	0=no 1=yes *	0=no 1=yes *	0=no 1=yes	0=no 1=yes	0=no 1=yes	0=no 1=yes	0=no 1=yes

*These status bits are appended to the corresponding data character in the FIFO. A read of the status register provides these bits (7:5) from the top of the FIFO together with bits 4:1. These bits are cleared by a 'reset error status' command. In character mode they are discarded when the corresponding data character is read from the FIFO.

TABLE I-4b DUART REGISTER BIT DESCRIPTIONS

	BIT7	BIT6	BIT5	BIT4	BIT3 BIT2	BIT1 BIT0
OPCR	OP7	OP6	OP5	OP4	OP3	OP2
	0=OPR[7] 1=TxRDYB	0=OPR[6] 1=TxRDYA	0=OPR[5] 1=RxRDY/ FFULLB	0=OPR[4] 1=RxRDY/ FULLA RS232	00=OPR[3] 01=C/T OUTPUT 10=TxCB(1X) 11=RxCB(1X)	00=OPR[2] 01=TxCA(16X) 10=TxCA(1X) 11=RxCA(1X)
	Must be 0	Must be 1	Must be 1	Must be 1	Must be 00	Must be 00

	BIT7	BIT6 BIT5 BIT4	BIT3	BIT2	BIT1	BIT0
ACR	BRG SET SELECT	COUNTER/TIMER MODE AND SOURCE	DELTA IP3 INT	DELTA IP2 INT	DELTA IP1 INT	DELTA IP0 INT
	0=set1 1=set2	See Table I-6	0=off 1=on Must be 1	0=off 1=on Must be 1	0=off 1=on Must be 1	0=off 1=on Must be 1

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IPCR	DELTA IP3	DELTA IP2	DELTA IP1	DELTA IP0	IP3	IP2	IP1	IP0
	0=no 1=yes	0=no 1=yes	0=no 1=yes	0=no 1=yes	0=low 1=high	0=low 1=high	0=low 1=high	0=low 1=high

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
ISR	INPUT PORT CHANGE	DELTA BREAK B	RxRDY/ FFULLB	TxRDYB	COUNTER READY	DELTA BREAK A	RxRDY/ FFULLA	TxRDYA
	0=no 1=yes	0=no 1=yes	0=no 1=yes	0=no 1=yes	0=no 1=yes	0=no 1=yes	0=no 1=yes	0=no 1=yes

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IMR	IN. PORT CHANGE INT	DELTA BREAK B INT	RxRDY/ FFULLB INT	TxRDYB INT	COUNTER READY INT	DELTA BREAK A INT	RxRDY/ FFULLA INT	TxRDYA INT
	0=off 1=on	0=off 1=on	0=off 1=on	0=off 1=on	0=off 1=on	0=off 1=on	0=off 1=on	0=off 1=on

CTUR	C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]

CTLR	C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]

8.9 CHANNEL A AND B MODE REGISTER ONE

A. MR1A - EIA RS232C MODE REGISTER

B. MR1B - KEYBOARD (SEND ONLY AUX. PRINTER) MODE REGISTER

8.9.1 MR1[7] MUST BE 0.

8.9.2 MR1[6] - Receiver Interrupt Select - This bit selects either the channel receiver ready status (RXRDY) or the channel A FIFO full status (FFULL) to be used for CPU interrupts. It also causes the selected bit to be output on OP4 if it is programmed as an interrupt output via the OPCR.

8.9.3 MR1[5] - Error Mode Select - This bit selects the operating mode of the three FIFO status bits (FE, PE, received break). In the "character" mode, status is provided on a character-by-character basis: the status applies only to the character at the top of the FIFO. In the "block" mode, the status provided in the SR for these bits is the accumulation (logical OR) of the status for all characters coming to the top of the FIFO since the last "reset error" command was issued.

8.9.4 MR1[4:3] - Parity Mode Select - If "with parity" or "force parity" is selected, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data.

8.9.5 MR1[2] - Parity Type Select - This bit selects the parity type (odd or even) if the "with parity" mode is programmed by MR1[4:3], and the polarity of the forced parity bit if the "force parity" mode is programmed. It has no effect if the "no parity" mode is programmed.

8.9.6 MR1[1:0] - Bits per Character Select - This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

8.10 CHANNEL A AND B MODE REGISTER TWO

A. MR2A - EIA RS232C MODE

B. MR2B - KEYBOARD (SEND ONLY AUX. PRINTER) MODE

8.10.1 MR2[7:6] - Mode Select - Each channel of the DUART can operate in one of four modes. MR2[7:6]=00 is the normal mode, with the transmitter and receiver operating independently. MR2[7:6]=01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxDA output.

2. The receive clock is used for the transmitter.

3. The receiver must be enabled, but the transmitter need not be enabled.

4. The TxRDY and TxEMT status bits are inactive.

5. The received parity is checked, but not regenerated for transmission, i.e., transmitted parity bit is as received.

6. Character framing is checked, but the stop bits are retransmitted as received.

7. A received break is echoed as received until the next valid start bit is detected.

8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

8.10.2 Two diagnostic modes can also be configured. MR2[7:6]=10 selects local loop-back mode. In this mode:

1. The transmitter output is internally connected to the receiver input.

2. The transmitter clock is used for the receiver.

3. The TxDA output is held high.

4. The RxDA input is ignored.

5. The transmitter must be enabled, but the receiver need not be enabled.

6. CPU to transmitter and receiver communications continue normally.

8.10.3 The second diagnostic mode is the remote loop-back mode, selected by MR2[7:6]=11. In this mode:

1. Received data is reclocked and retransmitted on the TxDA output.

2. The receive clock is used for the transmitter.

3. Received data is not sent to the local CPU, and the error status conditions are inactive.

4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity bit is as received.

5. The receiver must be enabled.

6. Character framing is not checked, and the stop bits are retransmitted as received.

7. A received break is echoed as received until the next valid start bit is detected.

8.10.4 The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is de-selected, the device will switch out of the mode immediately. An exception to this is switching out of auto-echo or remote loop-back modes: if the de-selection occurs just after the receiver has sampled the stop bit (indicated in auto-echo by assertion of RxRDY), and the transmitter is enabled the transmitter will remain in auto-echo mode until the entire stop bit has been retransmitted.

8.10.5 MR2[5] - MUST BE 0.

8.10.6 MR2[4] - MUST BE 0.

8.10.7 MR2[3:0] - Stop Bit Length Select - This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1-9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character length of 5 bits, 1-1/16 to 2 stop bits can be programmed in increments of 1/16 bit. The receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit if parity is enabled) in all cases.

8.11   CHANNEL A AND B CLOCK SELECT REGISTER

     A.   CSRA - EIA RS232C CLOCK SELECT REGISTER

     B.   CSRB - KEYBOARD (SEND ONLY AUX. PRINTER) CLOCK SELECT REGISTER

8.11.1 CSR[7:4] - Receiver Clock Select _ This field selects the baud rate clock for the receiver as follows:

Baud Rate
CLOCK=3.6864MHz

CSR[7:4]	ACR[7]=0	ACR[7]=1
0 0 0 0	50	75
0 0 0 1	110	110
0 0 1 0	134.5	134.5
0 0 1 1	200	150
0 1 0 0	300	300
0 1 0 1	600	600
0 1 1 0	1,200	1,200
0 1 1 1	1,050	2,000
1 0 0 0	2,400	2,400
1 0 0 1	4,800	4,800
1 0 1 0	7,200	1,800
1 0 1 1	9,600	9,600
1 1 0 0	38.4K	19.2K
1 1 0 1	Timer	Timer
1 1 1 0	DO NOT USE	DO NOT USE
1 1 1 1	DO NOT USE	DO NOT USE

8.11.2 The receiver clock is always a 16X clock.

8.11.3 CSR[3:0] – Transmitter Clock Select – This field selects the baud rate clock for the transmitter. The field definition is as per CSR[7:4].

8.11.4 The transmitter clock is always a 16X clock.

8.12 **CHANNEL A AND B COMMAND REGISTER**

A. CRA – EIA RS232C COMMAND REGISTER

B. CRB – KEYBOARD (SEND ONLY AUX PRINTER) COMMAND REGISTER

8.12.1 CR7 – MUST BE 0.

8.12.2 CR[6:4] – Miscellaneous Commands – The encoded value of this field may be used to specify a single command as follows:

CR[6:4]   COMMAND

0 0 0   No command.

0 0 1   Reset MR pointer. Causes the MR pointer to point to MR1.

0 1 0   Reset receiver. Resets the receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.

0 1 1   Reset transmitter. Resets the transmitter as if a hardware reset had been applied.

1 0 0   Reset error status. Clears the Received Break, Parity Error, Framing Error, and Overrun Error bits in the status registers (SRA[7:4]. Used in character mode and in block mode to clear all error status.

1 0 1   Reset break change interrupt. Causes the break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero.

1 1 0   Start break. Forces the TxD output low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the THR, the start of the break will be delayed until that character, or any others loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.

1 1 1   Stop break. The TxD line will go high (marking) within two bit times. TxD will remain high for one bit time before the next character, if any, is transmitted.

8.12.3 CR[3] – Disable Transmitter – This command terminates transmitter operation and resets the TxRDY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

8.12.4 CR[2] – Enable Transmitter – Enables operation of the transmitter. The TxRDY status bit will be asserted.

8.12.5 CR[1] – Disable Receiver – This command terminates operation of the receiver immediately – a character being received will be lost. The command has no effect on the receiver status bits or any other control registers.

8.12.6 CR[0] – Enable Receiver – Enables operation of the receiver. Forces the receiver into the search for start-bit state.

8.13 CHANNEL A AND B STATUS REGISTER

A. SRA – EIA RS232C STATUS

B. SRB – KEYBOARD (SEND ONLY AUX. PRINTER) STATUS

8.13.1 SR[7] - Received Break – This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received: further entries to the FIFO are inhibited until the RxD line returns to the marking state for at least one-half a bit time.

8.13.1.1 When this bit is set, the Delta Break bit in the ISR is set. ISR is also set when the end of the break condition, as defined above, is detected.

8.13.1.2 The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

8.13.2 SR[6] – Framing Error – This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

8.13.3 SR[5] – Parity Error – This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity.

8.13.4 SR[4] – Overrun Error – This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost. This bit is cleared by a 'reset error status' command.

8.13.5 SR[3] – Transmitter Empty (TxEMT) – This bit will be set when the transmitter underruns, i.e., both the transmit holding register (THR) and the transmit shift register are empty. It is set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU or when the transmitter is disabled.

8.13.6 SR[2] – Transmitter Ready (TxRDY) – This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled. Note! Characters loaded into the THR while the transmitter is disabled will not be transmitted.

8.13.7 SR[1] – FIFO Full (FFULL) – This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

8.13.8 SR[0] – Receiver Ready (RxRDY) – This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR, if after this read there are no more characters still in the FIFO.

8.14 OUTPUT PORT CONFIGURATION REGISTER (OPCR)

8.14.1 OPCR[7] – OP7 Output Select – This bit programs the OP7 output to provide the complement of OPR[7]. It must be '0'.

8.14.2 OPCR[6] – OP6 Output Select – This bit programs the OP6 output (INT232S) to provide the channel A transmitter interrupt output, which is the complement of TxRDYA. When in this mode OP6 acts as an open collector output. Note that this output is not masked by the contents of the IMR. It must be '1'.

8.14.3 OPCR[5] – OP5 Output Select – This bit programs the OP5 output (INTKBD) to provide the channel B receiver interrupt output, which is the complement of ISR[5]. When in this mode OP5 acts as an open collector output. Note that this output is not masked by the contents of the IMR. It must be '1'.

8.14.4 OPCR[4] – OP4 Output Select – This bit programs the OP4 output (INT232R) to provide the channel A receiver interrupt output, which is the complement of ISR 1]. When in this mode OP4 acts as an open collector output. Note that this output is not masked by the contents of the IMR. It must be '1'.

8.14.5 OPCR[3:2] – OP3 Output Select – This field programs the OP3 output to provide the complement of OPR[3]. It must be '1'.

8.14.6 OPCR[1:0] – OP2 Output Select – This field programs the OP2 output to provide the complement of OPR[2]. It must be '00'.

8.15 AUXILIARY CONTROL REGISTER (ACR)

8.15.1 ACR[7] - Baud Rate Generator Set Select - This bit selects one of two sets of baud rates to be generated by the BRG:

Set 1: 50, 110, 134.5, 200, 300, 600,
1.05K, 1.2K, 2.4K, 4.8K, 7.2K,
9.6K, and 38.4K baud.

Set 2: 75, 110, 134.5, 150, 300, 600,
1.2K, 1.8K, 2.0K, 2.4K, 4.8K,
9.6K, and 19.2K baud.

8.15.2 The selected set of rates is available for use by the channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in Table I-5.

TABLE I-5. BAUD RATE GENERATOR CHARACTERISTICS
CRYSTAL OR CLOCK=3.6864MHz

NOMINAL RATE(BAUD)	ACTUAL 16x CLOCK (kHz)	ERROR (PERCENT)
50	0.8	0
75	1.2	0
110	1.759	-0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	-0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2K	307.2	0
38.4K	614.4	0

NOTE: Duty cycle of 16X clock is 50% +/- 1%.

8.15.3 ACR[6:4] - Counter/Timer Mode and Clock Source Select- This field selects the operating mode of the counter/timer and its clock source as shown in Table I-6.

TABLE I-6. ACR[6:4] FIELD DEFINITION

ACR[6:4]	MODE	CLOCK SOURCE
0 0 0	Counter	IP2 is connected to the 30Hz video signal which has its transitions at the start of vertical blank.
0 0 1	Counter	TXCA-1X clock of channel A transmitter
0 1 0	Counter	TXCB-1X clock of channel B transmitter
0 1 1	Counter	3.6864MHz Crystal
1 0 0	Timer	(IP2) is connected to the 30Hz video signal which has its transitions at the start of vertical blank.
1 0 1	Timer	IP2 (see above) divided by 16.
1 1 0	Timer	3.6864MHz Crystal
1 1 1	Timer	3.6864MHz Crystal divided by 16

8.15.4 ACR[3:0] - IP3, IP2, IP1, IP0 Change of State Interrupt Enable - These must be '1' so the Input Port Change register (IPCR) cause the input change bit in the interrupt status register (ISR[7]) to be set. This results in the generation of an interrupt when mouse button 0, 1, or 2 (IP3, IP1, IP0) are pressed or released, or when video vertical blank starts (IP2).

8.16 INPUT PORT CHANGE REGISTER (IPCR)

8.16.1 Inputs IP3, IP1, IP0 are connected to mouse button 0, 1, and 3 respectively. Input IP2 is connected to a 60 Hz signal that has transitions at the start and end of vertical blank.

8.16.2 IPCR[7:4] - MB0, DOG CLK, MB1, MB2 Change of State - These bits are set when a change of state, as defined in the Input Port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register. The setting of these bits can be programmed to generate an interrupt to the CPU.

8.16.3 IPCR[3:0] - MB0, DOG CLK, MB1, MB2 Current State - These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

8.17 INTERRUPT STATUS REGISTER (ISR)

This register provides the status of all potential interrupt sources. The contents of this register are masked by the interrupt mask register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR - the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to 00 when the DUART is reset.

8.17.1 ISR[7] - Input Port Change Status - This bit is a '1' when a change of state has occurred at the MB2, MB1, DOG CLK, or MB0 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR. This bit indicates that a mouse button has been depressed or released or that vertical blank is starting.

8.17.2 ISR[6] - Channel B Change in Break - This bit, when set, indicates that the channel B receiver, which is connected to the keyboard, has detected the beginning or the end of a received break. It is reset when the CPU issues a channel B 'reset break change interrupt' command.

8.17.3 ISR[5] - Channel B Receiver Ready or FIFO Full - The function of this bit is programmed by MR1B[6]. If programmed as receiver ready, it indicates that a character has been received in channel B and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer causes the channel B FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

8.17.4 ISR[4] - Channel B Transmitter Ready - This bit indicates data can be sent to the keyboard or the auxiliary printer. This bit is a duplicate of TxRDYB (SRB[2]).

8.17.5 ISR[3] – Counter Ready – In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

8.17.5.1 In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/ timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

8.17.6 ISR[2] – Channel A Change in Break – This bit, when set, indicates that the channel A receiver, which is connected to the keyboard, has detected the beginning or the end of a received break. It is reset when the CPU issues a channel A 'reset break change interrupt' command.

8.17.7 ISR[1] – Channel A Receiver Ready or FIFO Full – The function of this bit is programmed by MR1A[6]. If programmed as receiver ready, it indicates that a character has been received in a channel A and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer causes the channel A FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

8.17.8 ISR[0] – Channel A Transmitter Ready – This bit indicates data can be sent to the EIA RS232C line. This bit is a duplicate of TxRDYA (SRA[2]).

8.18 INTERRUPT MASK REGISTER (IMR)

The programming of this register selects which bits in the ISR cause an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs INT232S, INTKBD, and INT232R or the reading of the ISR.

Normally this register would contain the following mask:

BIT		
7 = 1	Interrupt on mouse button change or vertical blank.
6 = 0	The keyboard should not cause a line break.
5 = 0	The keyboard receive data interrupt is handled by OPCR[5].
4 = 1	Interrupt when keyboard or auxiliary printer can receive data.
3 = 1	Interrupt when the programmed time out has occurred.
2 = 1	Interrupt when the EIA RS232C has a line break.
1 = 0	The EIA RS232C receive data interrupt is handled by OPCR[4].
0 = 0	The EIA RS232C send data interrupt is handled by OPCR[6].

8.19 COUNTER/TIMER REGISTERS (CTUR AND CTLR)

The CTUR and CTLR hold the eight MSB's and eight LSB's respectively of the value to be used by the counter/timer in either the counter or timer modes of operation. Note that these registers are write-only and cannot be read by the CPU.

8.19.1 In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half periods will be. In this mode the C/T runs continuously. Receipt of a start counter command (read address 20003B) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR.

8.19.2 The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read address 20003F). The command, however, does not stop the C/T.

8.19.3 In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching terminal count (0000), the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command. If new values have not been loaded, the previous count values are preserved and used for the next count cycle.

8.19.4 In the counter mode, the current value of the upper and lower 8 bits of the counter (CTU, CTL) may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8-bits to the upper 8-bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

8.20 FS-11 DESCRIPTION

8.20.1 DUART

8.20.1.1 MLA11 The DUART provides the interface between the I/O circuits and the processor. Data pins D0 - D7, address pins A0 - A3, enable pins GEN, WRN, RDN, and interrupt pins INTRN, INTKBD, INT232S allow the DUART to interrupt the processor and allow the processor to read ; 1 write the DUART. DUART pins MB2, MB1, MB0 interrupt the processor whenever a mouse button is released or depressed. DUART pin DOG CLK interrupts the processor whenever video vertical retrace blank starts and ends. DUART pin RVIDEO enables the processor to change the screen to either normal or reverse video.

8.20.2 Baud Rate Clock X1 supplies the DUART's internal baud rate generator with a clock from which the baud rates for the keyboard, auxiliary printer, and EIA RS232C lines are generated.

8.20.3 DUART Reset

8.20.3.1 MLE8-12 This pin provides power up reset to the DUART.

8.20.4 Keyboard Data Input Buffer

8.20.4.1 MLD6-9 This pin buffers the serial data from the keyboard to the DUART.

8.20.5 Keyboard, Auxiliary Printer Output Multiplexer

8.20.5.1 MLB9 Multiplex MLB9 directs the serial signal out of the DUART to the keyboard when OP3 is high and to the auxiliary printer when OP3 is low.

8.20.6 EIA Drivers

8.20.6.1 MLB8 This chip drives the EIA RS232C serial output signals and data terminal ready signals to the auxiliary printer and the EIA RS232C line to the host computer.

8.20.7 EIA Receivers

8.20.7.1 MLB6 This chip receives the EIA RS232C serial input, clear to send, data set ready and data carrier detect signals from the EIA RS232C line from the host computer.

9. FS-12 - EPROM AND SELECT LOGIC

EPROM's are used for storing programs called Firmware. A total of 8 (eight) 28 pin EPROM's may be installed. Each EPROM is organized into 8 bits per pack so it takes 4 EPROM's to make one 32 bit word. A selection switch allows 4 different memory packages to be inserted into the 8 EPROM sockets. The following list summarizes the different EPROM configurations.

1. 8K x 8 EPROM's can be inserted for 8K or 16K x 32 bits of firmware.

2. 8K x 8 RAM's can be inserted for 8K or 16K x 32 bits of firmware. The RAM's are used when developing firmware because it allows down loading into the firmware area.

3. 16K x 8 EPROM's can be inserted for 16K or 32K x 32 bits of firmware.

4. 32K x 8 EPROM's can be inserted for 32K or 64k x 32 bits of firmware.

Also, a switch option allows selection of 200nsec or 250nsec EPROM's. For a summary of the above information and switch positions necessary for each configuration see Figure I-4.

SWITCH NO.S	MEMORY CHIP TYPE & SIZE			
	8K X 8 RAM	8K X 8 ROM	16K X 8 ROM	32K X 8 ROM
1	ON	OFF	OFF	OFF
2	OFF	ON	OFF	OFF
3	OFF	OFF	ON	OFF
4	OFF	OFF	OFF	ON
5	OFF	ON	ON	OFF
6	OFF	OFF	OFF	ON

TOTAL MEMORY SIZE	CHIP LOCATIONS
8K X 32 (8K X 8 X 4)	F15, H15, J15, L15
16K X 32 (8K X 8 X 8)	F15, H15, J15, L15 F14, H14, J14, L14
16K X 32 (16K X 8 X 4)	F15, H15, J15, L15
32K X 32 (16K X 8 X 8)	F15, H15, J15, L15 F14, H14, J14, L4
32K X 32 (32K X 8 X 4)	F15 H15 J15 L15
64K X 32 (32K X 8 X 8)	F15, H15, J15, L15 F14, H14, J14, L14

MEMORY SPEED
≤ 200ns : SWITCH 8 ON
> 200ns : SWITCH 8 OFF

FIGURE I - 4

9.1 FS-12 DESCRIPTION

9.1.1 EPROM EPROM's MLL15, MLK15, MLH15, and MLG15 provide the low address bank of firmware.

EPROM's MLL14, MLK14, MLH14, and MLG14 provides the high address bank of firmware. The EPROM's are directly connected to the processor address and data busses.

9.1.2 EPROM Output Enable Control EPROM output enable (pin 22) onto the data bus is decoded by MLE7-6 (low address bank) and MLE7-3 (high address bank) when the processor addresses the EPROM. Multiplexer MLF15-9 and switches 2, 3, & 4 provide output enable selection for 8K, 16K, or 32K EPROMs.

9.1.3 EPROM Chip Enable Control EPROM chip enable (pin 20) is active whenever the processor address level 22 is low. This keeps the EPROM in the low power dissipation mode when the RAM is on and ready to do a fast data access when RAM is off.

9.1.4 EPROM Address Control EPROM address (pin 26) is connected to MLF15-7 which provides processor address level 15 used by 16K and 32K EPROMs. EPROM address (pin 27) is connected to MLF14-4, 7, 12, & 9 which provides processor address level 16 used by 32K EPROMs.

9.1.5 EPROM Fault Control MLF15-12 connects the write EPROM fault and watchdog timer fault circuits to the processor fault input.

9.1.6 EPROM Emulator Control Multiplexers MLF14 and MLF15 can be selected by closing switch 1 to provide operation of 8K x 8 static RAMs. MLF15 provides the signals to enable the RAMs and inhibit processor faults. MLF14 provides the signals to write the RAMs.

10. FS-13 - PARALLEL INTERFACE

10.1 OVERVIEW

The Parallel Interface is an 8 bit Parallel Input/Output port (PIO). It allows the BELLMAC 32A Processor to interface with an external I/O card. The external I/O card will be used to expand the I/O capability of the 5620.

In order to program the PIO you must know the programming requirements of the external I/O card connected to it. The PIO has control signals for addressing up to 32 external locations for either read or write operations. It also has two levels of interrupt priority and an asynchronous data ready signal that allows interfacing with I/O's much slower than the processor.

10.2 FS-13 DESCRIPTION

10.2.1 Parallel I/O Data Port

10.2.1.1 MLD8 This chip is a bidirectional eight bit data transceiver used to interface with an external I/O circuit boar

10.2.2 Parallel I/O Control Port

10.2.2.1 MLD7 This chip provides reset (pin 18), enable (pin 16), read/write (pin 14), address (pins 12, 9, 7, 5, 3), and MLD6-12 provides write control of the external I/O.

MLD6 provides input pins for interrupt (pins 4 and 6) and ready (pin 2) from the external I/O.

11. FS-14 - NONVOLATILE MEMORY (BATTERY BACK-UP RAM)

The Battery Back-Up RAM (BBRAM) is used for nonvolatile storage of terminal set up and configuration data. It has its own battery to prevent loss of data when the AC power is off. The organization of BBRAM is 2K x 8 bits. Its memory is read and written by the processor. Normal operation allows the user to configure the terminal options in a set-up mode and store this configuration in the BBRAM so the set-up process does not have to be repeated every time the terminal is powered up.

11.1 FS-14 DESCRIPTION

11.1.1 2K x 3 Static RAM

11.1.1.1 MLG13 This chip is the 2K x 8 static RAM used for storage of nonvolatile data. Signals MA121-MA021 are the address select lines from the processor. Signals MD151-MD081 are the 8 bit bidirectional data bus connected to the processor.

11.1.1.2 MLG13-21 Enables the static RAM for a write operation.

11.1.1.3 MLG13-20 Enables the static RAM outputs during a read operation.

11.1.1.4 MLG13-18 Enables the RAM for read and write operations when the power supply is on. This signal is held active (low) by transistor Q1 as long as dc power is within its specified range.

11.1.2 Battery Recharging Circuit Resistors R4, R5, R6, diodes CR1, CR2, and capacitors C1, C2 are used to generate a battery isolated and filtered +5 volts from the +5 volt and +12 volt supplies. Resistor R11 and diode CR5 recharge the battery when power is on. When the power is turned off battery B1 resistor R7 and diode CR6 are used to maintain data in the RAM by supplying voltage to

MLG13-24, while MLG13-18 disables read/write operations.

12. FS-15 - POWER DISTRIBUTION

DCOK1 is a reset signal from the power supply. It is on for a minimum of one milli-second after the voltages are in range and before the voltages go out of range.

The +12V, +5V, and -12V are power lines from the logic power supply. Nominal current levels are as follows:

DC Voltage	DC Current	DC power
+5	3.0A	15 Watts
+12	130mA	1.56 Watts
-12	90mA	1.08 Watts

NOTE: MANUFACTURE PER MR 2001 AND MR 2029 GROUP 4

REVISIONS — SHEET 2

	CUSTOMER IDENTIFICATION ISSUE	TYPE VERSION	ASSOCIATED NOTE	DRAWING ISSUE	CONFORMANCE DATE	AUTH. NO.
1	I	A	—	1	6-29-84	28734R
2	I	A	—	2	11-26-84	28497
3	I	B	—	3	2-18-85	28205
4	I	C	—	4	2-18-85	29390

HAND STAMP 128

410 — ASM ISS

SEE EQUIPMENT NOTE 102 FOR EXACT LOCATION OF CR7 AND CR8

407715 CONNECTOR W/340158 RIVET (2 PLS)

SEE EQUIPMENT NOTE 102 FOR EXACT LOCATION OF CR9 AND CR10

452179 LABEL AFFIXED TO BOARD UNDER BATTERY.

405037 CONNECTOR W/405184 PINS IN POSITIONS 1,2,3,4,6

401624 CONNECTOR W/341644 PINS (9 PLS)

409472 ETCHED CIRCUIT BOARD

412418 SOCKET (8 PLS)

CIRCUIT CARD

MC

TERMINAL LOGIC CARD ASSEMBLY

APPROVALS

PROJ. SUPV. / PROJ. DIR. / MFG. REL. COMPL.

ENGR. DCZ   DSGNR.

DRAWN JLO   DATE 4-25-84

E-NUMBER 410128

SD-CD NO. 4972

R & D FILE NO. 3-A185.234A

TELETYPE CORPORATION

410128   (1 OF 2)

SIMILAR TO:

TC661-0579

Parts List — Column 1

REF. DESIG.	PART NO. REQ	DESCRIPTION
MLA2	474161	IC, 4-BIT SYNC COUNTER
MLA5-A8		SAME AS MLA2
MLA11	404381	IC, DUART
MLA12	474032	IC, QUAD 2-INPUT OR
MLA13	411405	IC, OSC. 32.77324 MHz
MLA15	374C96	IC, QUAD 2-INPUT XOR
MLB3-B4		SAME AS MLA2
MLB6	335529	IC, EIA LINE RECEIVER
MLB8	335528	IC, EIA LINE DRIVER
MLB9	474000	IC, QUAD 2-INPUT NAND
MLB12	374020	IC, DUAL 4-INPUT NAND
MLB13	NOTE 104	IC, CLOCK OSC. 28.8 MHz
MLB15	NOTE 104	IC, BELLMAC 32A
MLC2	474109	IC, JK FLIP FLOP
MLC3	416512	IC, VERT. ROM, 512 X 8
MLC4	416513	IC, HORIZ. ROM 512 X 8
MLC5	474374	IC, OCTAL D FLIP FLOP
MLC6	416531	IC, HOUSE PAL
MLC7	474569	IC, COUNTER
MLC8		SAME AS MLC7
MLC9		SAME AS MLC6
MLC10	474021	IC, DUAL 4-INPUT NAND
MLC11	474002	IC, QUAD 2-INPUT NOR
MLC12	474138	IC, 3 TO 8 DECODER
MLC13	339353	IC, 4 BIT COUNTER
MLD2-D3		SAME AS MLC5
MLD4-D5		SAME AS MLC7
MLD6	474244	IC, OCTAL BUFFER
MLD7		SAME AS MLD6
MLD8	474245	IC, TRANSCEIVER
MLD9	374244	IC, OCTAL BUFFER, FAST
MLD11		SAME AS MLC10
MLD12		SAME AS MLD6
MLD13	404195	IC, 4 BIT SHIFT REGISTER
MLE1	374002	IC, QUAD 2-INPUT NOR
MLE2-E5		SAME AS MLA2
MLE6	474253	IC, 4 TO 1 MULTIPLEXER
MLE7		SAME AS MLA12
MLE8	474004	IC, HEX INVERTER
MLE9		SAME AS MLA2
MLF1	374032	IC, QUAD 2-INPUT OR
MLF2	339166	IC, 8 BIT SHIFT REGISTER
MLF3-F5		SAME AS MLF2
MLF6-F9		SAME AS MLE6
MLF14	374257	IC, MULTIPLEXER
MLF15		SAME AS MLF14
MLG1	474008	IC, QUAD 2-INPUT AND
MLG2-G5		SAME AS MLC5
MLG6-G8		SAME AS MLD9
MLG9	474373	IC, TRANSPARENT LATCH
MLG13	404411	IC, 2KX8 STAT CMOS RAM
MLG14	NOTE 105	IC, EPROM 8K X 8
MLG15	NOTE 105	IC, EPROM 8K X 8
MLH1		SAME AS MLC2
MLH2	374000	IC, QUAD 2-INPUT NAND
MLH3	474010	IC, TRIPLE 3-INPUT NAND
MLH5	404256	IC, 256K RAM MEMORY

Parts List — Column 2

REF. DESIG.	PART NO. REQ	DESCRIPTION
MLH6-H8		SAME AS MLH5
MLH10-13		SAME AS MLH5
MLH14	NOTE 105	IC, EPROM 8K X 8
MLH15	NOTE 105	IC, EPROM 8K X 8
MLJ1	374109	IC, DUAL JK FLIP FLOP
MLJ2		SAME AS MLE1
MLJ5-J8		SAME AS MLH5
MLJ9		SAME AS MLG9
MLJ10-13		SAME AS MLH5
MLK1		SAME AS MLJ1
MLK2		SAME AS MLH2
MLK3		SAME AS MLE8
MLK5-K8		SAME AS MLH5
MLK9		SAME AS MLG9
MLK10-13		SAME AS MLH5
MLK14	NOTE 105	IC, EPROM 8K X 8
MLK15	NOTE 105	IC, EPROM 8K X 8
MLL2	374161	IC, 4 BIT COUNTER
MLL3		SAME AS MLD13
MLL5-L8		SAME AS MLH5
MLL9		SAME AS MLG9
MLL10-13		SAME AS MLH5
MLL14	NOTE 105	IC, EPROM 8K X 8
MLL15	NOTE 105	IC, EPROM 8K X 8
Q1	333241	TRANSISTOR 2N4401-5
CR1-10	197464	DIODE 1N4148
RP1	341733	RESISTOR PKG. 6.8K Ω
RP2-5	453910	RESISTOR PKG. 100 Ω
R1	411258	RESISTOR 4.7K Ω
R2	411274	RESISTOR 22K Ω
R3	411256	RESISTOR 10K Ω
R4-6	182180	RESISTOR 200Ω/2.1

Parts List — Column 3

REF. DESIG.	PART NO. REQ	DESCRIPTION
R7	411211	RESISTOR 51 Ω
R8	411242	RESISTOR 1K Ω
R9-10		SAME AS R3
R11	411238	RESISTOR 680 Ω
R12		SAME AS R3
BAT 1	406099	BATTERY, 3.6V NICAD
X1	416511	CRYSTAL, 3.6864 MHz
C1	337334	CAPACITOR 6.8uF
C2	405324	CAPACITOR .1uF
C3-6	335800	CAPACITOR 330pF
C7	335803	CAPACITOR 220pF
C8-10	346729	CAPACITOR 1200pF
C11	346351	CAPACITOR 10pF
C12-22	310931	CAPACITOR 47uF
C23-115		SAME AS C2
C117-144		SAME AS C2
J1	405037	CONNECTOR, 6 PIN
J2	407715	CONNECTOR, 50 PIN
J3	401624	CONNECTOR, 9 PIN
	405184	TERMINAL, P.C.
	341644	TERMINAL, P.C.
	409972	BOARD, CIRCUIT
OS1	341808	8 PCS, DIP SWITCH
STP1	336470	STRAP
STP2		SAME AS STP1
	412416	SOCKET, 16 PIN
	412418	SOCKET, 28 PIN
	340158	RIVET
	452179	LABEL, INSTRUCTION

EQUIPMENT NOTES

101. THE SMALL CIRCLES WITHIN THE COMPONENT OUTLINE ON THE SILK SCREEN INDICATE: PIN 1 OF ALL IC's OR, THE POSITIVE LEAD ON POLARIZED DISCRETE COMPONENTS.

102. THE I/O FILTER CARD MUST HAVE FOUR DIODES TO PROTECT MLC6 & MLC9 FROM ELECTRO-STATIC DISCHARGE. THE ANODES ARE CONNECTED TO X0, X1, Y0, Y1 AND THE CATHODES ARE CONNECTED TO +5 VOLTS.

103. THE 410128 CARD IS THE SAME AS THE 410972 CARD EXCEPT FOR THE DYNAMIC RAM AND THEIR SOCKETS. 4972SD AND 4972CO REFER TO BOTH 410128 AND 410972.

104. THE 410128 MAY BE EQUIPPED WITH ONE OF TWO DIFFERENT PROCESSORS:

404132 PROCESSOR:
MLB13 – 416514 IC CLOCK OSCILLATOR 28.8 MHz
MLB15 – 404132 IC BELLMAC 32A CPU

410962 PROCESSOR:
MLB13 – NO PART
MLB15 – 410962 IC BELLMAC 32B CPU CARD ASM.

105. NOTE THE FIRMWARE VERSION MUST BE COMPATIBLE WITH THE PROCESSOR USED ON THE CARD. SEE NOTE 104.

VERSION	COMPATIBLE	MLG14	MLG15	MLH14	MLH15	MLK14	MLK15	MLL14	MLL15	OS3 O-OPEN C-CLOSED 1 2 3 4 5 6 7 8
8;7;1	32A CPU	416523	416524	416525	416526	416527	416528	416529	416530	O C O O C O O C
8;7;2	32A CPU	416866	416867	416868	416869	416870	416871	416872	416873	O C O O C O O C
8;7;3	32A CPU	416904	416905	416906	416907	416908	416909	416910	416911	O C O O C O O C
8;7;3	32A CPU	416955	416956	416957	416958	416959	416960	416961	416962	O C O O C O O C
8;7;3	32A/32B CPU	456780	456781	456782	456783	456784	456785	456786	456787	O C O O C O O C

REVISIONS

CUSTOMER IDENTIFICATION ISSUE	MFG VERSION	ASSOCIATED NOTE	DRAWING ISSUE	CONFORMANCE DATE	AUTH. NO.
I	A	—	1	6-29-84	28734R
			2		
			3		
			4		

Circuit Card Assembly drawing — Terminal Logic Card Assembly, Teletype Corporation, drawing 410972 (1 of 2).

NOTE: MANUFACTURE PER MR2001 AND MR2029 GROUP 4

STAMP IN LAST THREE DIGITS (972)

410 ASM.ISS.

SEE EQUIPMENT NOTE 102 FOR EXACT LOCATION OF CR7 & CR8.

407715 CONNECTOR W/340158 RIVET (2 PLS)

SEE EQUIPMENT NOTE 102 FOR EXACT LOCATION OF CR9 & CR10

405037 CONNECTOR W/405184 PINS IN POSITIONS 1, 2, 3, 4, 6

401624 CONNECTOR W/341644 PINS (9 PLS)

409472 ETCHED CIRCUIT BOARD

ML815 SPACED .062 ABOVE CARD WHEN SOLDERING

412418 SOCKET (8 PLS)

412418 SOCKET (32 PLS)

452179 LABEL AFFIXED TO BOARD UNDER BATTERY.

SIMILAR TO:

TC661-0679

SHEET 2	CUSTOMER IDENTIFICATION ISSUE	MFG VERSION	ASSOCIATED NOTE	DRAWING ISSUE	CONFORMANCE DATE	AUTH. NO.
1	1	A	—	1	9-9-83	28057R
2	2	A	102	2	1-19-84	27540
3	2	B	—	3	—	27793
4	3	A	103	4	2-21-84	27814
5	4	A	104	5	5-30-84	27923
6	4	A	—	6	—	28110
7	5	A	106	7	12-7-84	28107
8	5	B	—	9	2-18-85	28205
9	5	C	—	9	2-18-85	28390

REF. DESIG.	PART NO. REQ.	DESCRIPTION
MLA2	474161	IC, 4-BIT SYNC COUNTER
MLA5-A6		SAME AS MLA2
MLA11	404381	IC, UART
MLA12	474032	IC, QUAD 2-INPUT OR
MLA13	411405	IC, OSC. 32.77824 MHz
MLA15	374086	IC, QUAD 2-INPUT XOR
MLB3-B4		SAME AS MLA2
MLB6	335529	IC, EIA LINE RECEIVER
MLB8	335528	IC, EIA LINE DRIVER
MLB9	474000	IC, QUAD 2-INPUT NAND
MLB12	374020	IC, DUAL 4-INPUT NAND
MLB13	NOTE 104	IC, CLOCK OSC. 28.8 MHz
MLB15	NOTE 104	IC, BELLMAC 32A
MLC2	474109	IC, JK FLIP FLOP
MLC3	416512	IC, VERT. ROM, 512 X 8
MLC4	416513	IC, HORIZ. ROM 512 X 8
MLC5	474574	IC, OCTAL D FLIP FLOP
MLC6	416531	IC, MOUSE PAL
MLC7	474569	IC, COUNTER
MLC8		SAME AS MLC7
MLC9		SAME AS MLC5
MLC10	474021	IC, DUAL 4-INPUT NAND
MLC11	474002	IC, QUAD 2-INPUT NOR
MLC12	474138	IC, 3 TO 8 DECODER
MLC13	339363	IC, 4 BIT COUNTER
MLD2-D3		SAME AS MLC5
MLD4-D5		SAME AS MLC7
MLD6	474244	IC, OCTAL BUFFER
MLD7		SAME AS MLD6
MLD8	474245	IC, TRANSCEIVER
MLD9	374244	IC, OCTAL BUFFER, FAST
MLD11		SAME AS MLC10
MLD12		SAME AS MLD6
MLD13	404195	IC, 4 BIT SHIFT REGISTER
MLE1	374002	IC, QUAD 2-INPUT NOR
MLE2-E5		SAME AS MLA2
MLE6	474253	IC, 4 TO 1 MULTIPLEXER
MLE7		SAME AS MLA12
MLE8	474004	IC, HEX INVERTER
MLE9		SAME AS MLA2
MLF1	374032	IC, QUAD 2-INPUT OR
MLF2	339166	IC, 8 BIT SHIFT REGISTER
MLF3-F5		SAME AS MLF2
MLF6-F9		SAME AS MLE6
MLF14	374257	IC, MULTIPLEXER
MLF15		SAME AS MLF14
MLG1	474008	IC, QUAD 2-INPUT AND
MLG2-G5		SAME AS MLC5
MLG6-G8		SAME AS MLD9
MLG9	474373	IC, TRANSPARENT LATCH
MLG13	404417	IC, 2KX8 STAT CMOS RAM
MLG14	NOTE 105	IC, EPROM 8K X 8
MLG15	NOTE 105	IC, EPROM 8K X 8
MLH1		SAME AS MLC2
MLH2	374000	IC, QUAD 2-INPUT NAND
MLH3	474010	IC, TRIPLE 3-INPUT NAND
MLH5	404164	IC, 256K RAM MEMORY

REF. DESIG.	PART NO. REQ.	DESCRIPTION
MLH6-H8		SAME AS MLH5
MLH10-13		SAME AS MLH5
MLH14	NOTE 105	IC, EPROM 8K X 8
MLH15	NOTE 105	IC, EPROM 8K X 8
MLJ1	374109	IC, DUAL JK FLIP FLOP
MLJ2		SAME AS MLE1
MLJ5-J8		SAME AS MLH5
MLJ9		SAME AS MLG9
MLJ10-13		SAME AS MLH5
MLK1		SAME AS MLJ1
MLK2		SAME AS MLJ2
MLK3		SAME AS MLE8
MLK5-K8		SAME AS MLH5
MLK9		SAME AS MLG9
MLK10-13		SAME AS MLH5
MLK14	NOTE 105	IC, EPROM 8K X 8
MLK15	NOTE 105	IC, EPROM 8K X 8
MLL2	374161	IC, 4 BIT COUNTER
MLL3		SAME AS MLD13
MLL5-L8		SAME AS MLH5
MLL9		SAME AS MLG9
MLL10-13		SAME AS MLH5
MLL14	NOTE 105	IC, EPROM 8K X 8
MLL15	NOTE 105	IC, EPROM 8K X 8
Q1	333241	TRANSISTOR 2N4401-5
CR1-6	197464	DIODE 1N4148
RP1	341733	RESISTOR PKG. 6.8K Ω
RP2-5	453910	RESISTOR PKG. 100 Ω
R1	411258	RESISTOR 4.7K Ω
R2	411274	RESISTOR 22K Ω
R3	411266	RESISTOR 10K Ω
R4-6	182180	RESISTOR 200 Ω /2W

REF. DESIG.	PART NO. REQ.	DESCRIPTION
R7	411211	RESISTOR 51 Ω
R8	411242	RESISTOR 1K Ω
R9-10		SAME AS R3
R11	411239	RESISTOR 680 Ω
R12		SAME AS R3
BAT1	406099	BATTERY, 3.6V NICAD
X1	416511	CRYSTAL, 3.6864 MHz
C1	335334	CAPACITOR 6.8µF
C2	405324	CAPACITOR .1µF
C3-6	335800	CAPACITOR 330pF
C7	335803	CAPACITOR 220pF
C8-10	346729	CAPACITOR 1200pF
C11	346351	CAPACITOR 10pF
C12-22	310931	CAPACITOR 47µF
C23-115		SAME AS C2
C117-144		SAME AS C2
J1	405037	CONNECTOR, 6 PIN
J2	407715	CONNECTOR, 50 PIN
J3	401624	CONNECTOR, 9 PIN
	405184	TERMINAL, P.C.
	341644	TERMINAL, P.C.
	409972	BOARD, CIRCUIT
OS1	341808	8 PCS. DIP SWITCH
STP1	336470	STRAP
STP2		SAME AS STP1
	412416	SOCKET, 16 PIN
	412418	SOCKET, 28 PIN
	340158	RIVET
	452179	LABEL, INSTRUCTION

EQUIPMENT NOTES

101. THE SMALL CIRCLES WITHIN THE COMPONENT OUTLINE ON THE SILK SCREEN INDICATE: PIN 1 OF ALL IC's OR, THE POSITIVE LEAD ON POLARIZED DISCRETE COMPONENTS.

102. THE I/O FILTER CARD MUST HAVE FOUR DIODES TO PROTECT MLC6 & MLC9 FROM ELECTRO-STATIC DISCHARGE. THE ANODES ARE CONNECTED TO X0, X1, Y0, Y1 AND THE CATHODES ARE CONNECTED TO +5 VOLTS.

103. IF THE 410972 CARD WAS MODIFIED PER MODIFICATION KIT 416563 TO PROVIDE A MEGABYTE OF RAM, THE THIRTY TWO/8 PIN SOCKETS WILL HAVE 256K RAM MEMORY IC's (TPN 404256).

104. THE 410972 MAY BE EQUIPPED WITH ONE OF TWO DIFFERENT PROCESSORS:

　　404132 PROCESSOR:
　　　MLB13-416514 IC CLOCK OSCILLATOR 28.8 MHz
　　　MLB15-404132 IC BELLMAC 32A CPU

　　410862 PROCESSOR:
　　　MLB13-NO PART
　　　MLB15-410862 IC BELLMAC 32B CPU CARD ASM.

105. NOTE THE FIRMWARE VERSION MUST BE COMPATIBLE WITH THE PROCESSOR USED ON THE CARD. SEE NOTE 104.

VERSION	COMPATIBLE	MLG14	MLG15	MLH14	MLH15	MLK14	MLK15	MLL14	MLL15	OS1 OPEN O CLOSED 1 2 3 4 5 6 7 8
8;7;1	32A CPU	416523	416524	416525	416526	416527	416528	416529	416530	OC OO C OOC
8;7;2	32A CPU	416866	416867	416868	416869	416870	416871	416872	416873	OC OO C OOC
8;7;3	32A CPU	416904	416905	416906	416907	416908	416909	416910	416911	OC OO C OOC
8;7;3	32A CPU	416955	416956	416957	416958	416959	416960	416961	416962	OC OO C OOC
8;7;3	32A/32B CPU	456780	456781	456782	456783	456784	456785	456786	456797	OC OO C OOC

106. A 374161 AT MLL2 GUARANTEES TIMING FOR 256K DYNAMIC RAMS (404256).

REVISIONS

			ASSOCIATED NOTE	
			6	
			7	
			8	
			9	

CIRCUIT CARD

TERMINAL LOGIC CARD ASSEMBLY

APPROVALS

ENGR. DCL
DATE 4-25-84
SD-CD NO. 4972
R & D FILE NO. 3-A185.234A

SHEET INDEX

CONTENTS	SHEET NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	SHEET NO.
SHEET INDEX	A1	1	2	3	4																									A1
FS-1 BELLMAC 32 PROCESSOR	B1	1	2	2	2																									B1
FS-2 DRAM BYTE 0	B2	1	1	1	1																									B2
FS-3 DRAM BYTE 1	B3	1	1	1	1																									B3
FS-4 DRAM BYTE 2	B4	1	1	1	1																									B4
FS-5 DRAM BYTE 3	B5	1	1	1	1																									B5
FS-6 MEMORY ARBITER	B6	1	2	3	3																									B6
FS-7 DISPLAY TIMING	B7	1	1	1	1																									B7
FS-8 DISPLAY ADDRESS	B8	1	1	1	1																									B8
FS-9 VIDEO TIMING & SHIFT REGISTERS	B9	1	1	1	1																									B9
FS-10 MOUSE DECODING	B10	1	2	2	3																									B10
FS-11 KEYBOARD & EIA INTERFACES	B11	1	1	1	1																									B11
FS-12 EPROM & SELECT LOGIC	B12	1	2	2	2																									B12
FS-13 PARALLEL INTERFACE	B13	1	1	1	1																									B13
FS-14 NON-VOLATILE MEMORY	B14	1	1	1	1																									B14
FS-15 POWER DISTRIBUTION	B15	1	1	1	1																									B15
FS-16 SPARE FUNCTIONS	B16	1	1	1	1																									B16
INFORMATION & SCHEMATIC NOTES	D1	1	1	1	1																									D1
INFORMATION & SCHEMATIC NOTES	D2	1	2	2	2																									D2
PROCESSOR TIMING 404132 (32A)	E1	1	2	2	2																									E1
DYNAMIC RAM TIMING	E2	1	1	1	1																									E2
MOUSE TIMING	E3	1	1	1	1																									E3
DISPLAY TIMING	E4	1	1	1	1																									E4
VIDEO TIMING	E5	1	1	1	1																									E5
PROCESSOR TIMING 410862 (32B)	E6	-	1	1	1																									E6
BD-1 BLOCK DIAGRAM	H1	1	1	1	1																									H1

SUPPORTING INFORMATION

CATEGORY	NO.
ASSEMBLY DRAWING	410972
SCHEMATIC DIAGRAM	4973SD
CIRCUIT DESCRIPTION	4972CD
ASSEMBLY DRAWING	410862
SCHEMATIC DIAGRAM	4862SD
CIRCUIT DESCRIPTION	4862CD
ASSEMBLY DRAWING	410128

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND UPDATED EACH TIME ANY SHEET OF THE DRAWING IS REISSUED OR A NEW SHEET IS ADDED.
3. THE LAST COMPLETED COLUMN INDICATES THE LATEST ISSUE NUMBER OF THE SHEET INDEX.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NO.
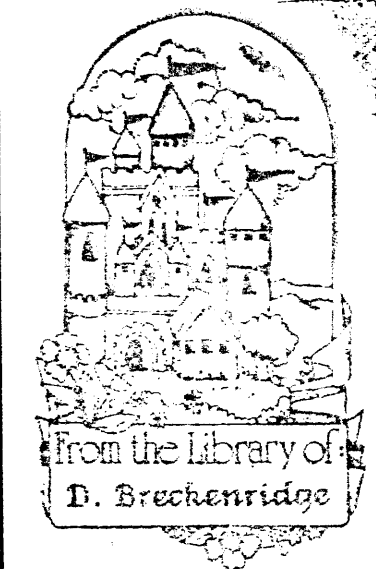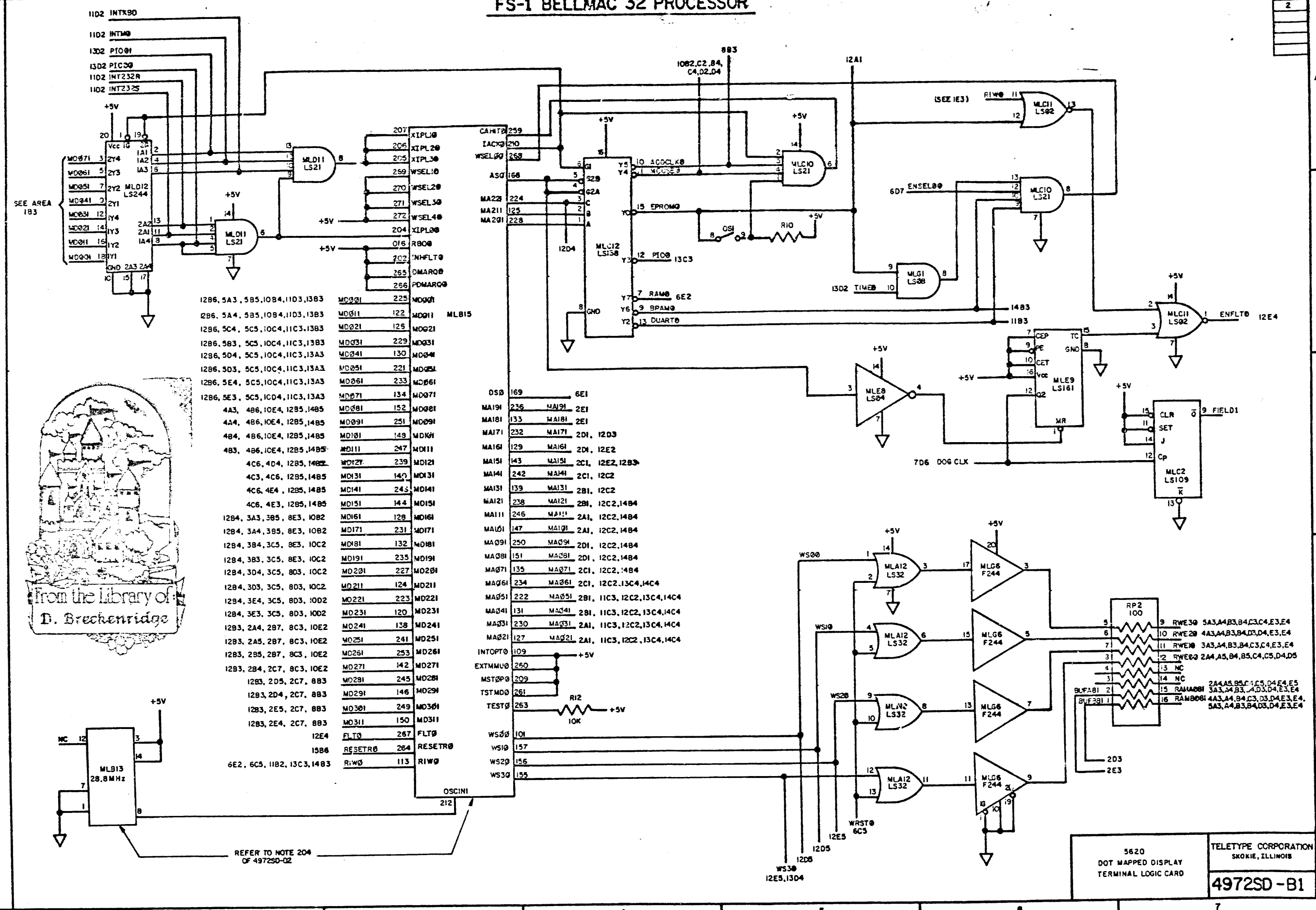5. ISSUE DATES WILL BE SHOWN ON THE SHEET INDEX ONLY.

TC 641 (3-69)

FS-1 BELLMAC 32 PROCESSOR

TELETYPE CORPORATION
SKOKIE, ILLINOIS

5620
DOT MAPPED DISPLAY
TERMINAL LOGIC CARD

4972SD -B1

686 RAS3Q
686 CAS3Q

6AI SELI
6D4 DQI

DO24I 9A3
DO25I 9B3
DO26I 9D3
DO27I 9E3
DO28I 9A3
DO29I 9C3
DO3OI 9D3
DO3II 9E3

MUXOI 4CI
MUXII 4CI
MUX2I 4CI
MUX3I 4CI
MUX5I 4CI
MUX4I 4CI
MUX6I 4CI
MUX7I 4CI

BUFB8I ID6
BUFA8I ID6

MLE8 LS253
MLF6 LS253
MLF7 LS253
MLF8 LS253
MLF9 LS253
MLG8 F244
MLG6 F244

RP4 100

MLL5 RAM
MLL6 RAM
MLL7 RAM
MLL8 RAM
MLL1O RAM
MLL11 RAM
MLL12 RAM
MLL13 RAM
MLL9 LS373

PENØ 6E4
PLOADI 6C2

MD24I
MD25I
MD26I
MD27I
MD28I
MD29I
MD3OI
MD3II

5620
DOT MAPPED DISPLAY
TERMINAL LOGIC CARD

TELETYPE CORPORATION
SKOKIE, ILLINOIS

4972SD-B2

TC640-O78I

FS-3 DRAM BYTE I

5620
DOT MAPPED DISPLAY
TERMINAL LOGIC CARD

TELETYPE CORPORATION
SKOKIE, ILLINOIS

4972SD-B3

TC640-0781

FS-4 DRAM BYTE 2

TELETYPE CORPORATION
SKOKIE, ILLINOIS

5620
DOT MAPPED DISPLAY
TERMINAL LOGIC CARD

4972SD-B4

FS-5 DRAM BYTE 3

TC640-0781

FS-6 MEMORY ARBITER

FS-7 DISPLAY TIMING

FS-8 DISPLAY ADDRESS

TC640-0791

FS-9 VIDEO TIMING & SHIFT REGISTERS

ISSUE

FS-10 MOUSE DECODING

FS-11 KEYBOARD & EIA INTERFACES

J2

4 +5V
1 -12V
3 MS_OUT

9 MLD6 11
LS244

3 ML89 8   4 MLB9 6
10 LS00   5 LS00   +5V 14

2 MS_IN
5 GND

9E6 RVIDEO

12 MLB9 11   1 MLB9 3
13 LS00   2 LS00 7

IC9   DOGCLK 36 OPI 12
                  IP2

10A6 1A2 7 IP0   RxDb 10
10A6 M81 4 IP1   TxDb 11
10A5 M80 2 IP3   OP3 13
1B6 DLART0 35 CEN
1E3 R1W0 8 WRN
14A5 R0W1 9 RDN

1D4 MA051 6 A3   MLA11
1D4 MA041 5 A2   SC2681
1D4 MA031 3 A1
1D4 MA021 1 A0

C11
10pF

OP7 15
OP0 29
TxDa 30

2 1A   1Y 3   26 AUXENC
4 2A   2Y 6   25 AUXDTRC
9 3A   3Y 8   15 DTRC
12 4A   4Y 11   22 TXDRSC
5 2B   MLB8 DR
10 3B   75188
4B GND-Vcc+Vcc
13 7 1 14

X1 3.6864MHz CRYSTAL
X1CLK 32 X1/CLK
X2CLK 33 X2
STP1

C6 330pF C5 330pF C4 330pF C3 330pF

CR3   +12V
CR4   -12V

+5V

MD071 19 D7
MD061 22 D6
MD051 18 D5
MD041 21 D4
MD031 17 D3
MD021 24 D2
MD011 16 D1
MD001 25 D0

1B3

RPI 6.8K

RxDa 31   3 1Y   1A 1   21 RXDRSC
IP4 39   6 2Y   2A 2   23 CTSC
IP5 38   8 3Y   3A 10 18 DSRC
IP6 37   11 4Y   4A 13 19 DCDC
           14 Vcc 3A
+5V   MLB6 RCV
           75189
           2 1C   4C 12
           2C   3C 9

21 INTRN
27 OP4
14 OP5
25 OP6
GND Vcc RESET1
20 40 34

INTM0 1A2
INT232R 1A2
INTK80 1A2
INT232S 1A2

RESETR1 1586

+5V

12
MLE8 LS04
13

RESETR0 1586

C7 220pF C8 220pF C9 220pF C10 220pF

+5V   16 Vcc
+12V   20 +12V
-12V   17 -12V
       24 GND

5620
DOT MAPPED DISPLAY
TERMINAL LOGIC CARD

TELETYPE CORPORATION
SKOKIE, ILLINOIS

4972SD-B11

TC640-0781

FS-12 EPROM AND SELECT LOGIC

PROGRAMMING OF OS1

SWITCH POS NO.	MEMORY TYPE			
	8K RAM	8K ROM	16K ROM	32K ROM
1	C	O	O	O
2	O	C	O	O
3	O	O	C	O
4	O	O	O	C
5	O	C	C	C
6	O	O	O	C
7	O	O	O	O
8	C	C	C	O

C = CLOSED / O = OPEN

TC640-0781

FS-13 PARALLEL INTERFACE

+5V
20
Vcc

J2

MLD8 LS245

MOO71	11	B8	A8	9	33 PIDO7I
MOO61	12	B7	A7	8	38 PIDO6I
MOO51	13	B6	A6	7	37 PIDO5I
MOO41	14	B5	A5	6	42 PIDO4I
MOO31	15	B4	A4	5	41 PIDO3I
MOO21	16	B3	A3	4	46 PIDO2I
MOO11	17	B2	A2	3	45 PIDO1I
MOO01	18	B1	A1	2	50 PIDO0I

I83

OC 19   DIR 1   GND 10

MLD7 LS244

I586 RESETR0	2	1A1	1Y1	18	49 PIORST0
I84 PIO0	4	1A2	1Y2	16	48 PIOEN0
IE3 RIW0	6	1A3	1Y3	14	47 PIOWEN0
MAO21	8	1A4	1Y4	12	44 ADDRO21
MAO31	11	2A1	2Y1	9	43 ADDRO1I
MAO41	13	2A2	2Y2	7	40 ADDRO21
MAO51	15	2A3	2Y3	5	39 ADDRO51
MAO61	17	2A4	2Y4	3	36 ADDRO41

I04

GND 10   Vcc 20   1G 1   2G 19

+5V

RP1 6.8K
+5V

TO/ FROM PARALLEL PORT

27 PORTEN0

MLD6 LS244

I85 TIME0	18	1Y1	1A1	2	35 TIME
IA2 PIO00	16	1Y2	1A2	4	32 INT0
IA_ PIO01	14	1Y3	1A3	6	31 INT1
IE5 WS30	8	1A4	1Y4	12	28 STROBE0

GND 10   Vcc 20
+5V

+5V ——— 30 +5V
+12V ——— 29 +12V
−12V ——— 34 −12V

FS-14 NON VOLATILE MEMORY

MLE8 LS04 5 6

ROWI 6D5

IE3 RIW0 9
I86 BRAM0 10
MLE7 LS032 8 21 $\overline{WE}$
20 $\overline{OE}$

13 MLE7 LS032 11
12

IC3

MLG13
404417
2K X 8
SRAM

MAI2I	19	A10
MAIII	22	A9
MAI0I	23	A8
MA09I	1	A7
MA08I	2	A6
MA07I	3	A5
MA06I	4	A4
MA05I	5	A3
MA04I	6	A2
MA03I	7	A1
MA02I	8	A0

I/08	17	MD15I
I/07	16	MD14I
I/06	15	MD13I
I/05	14	MD12I
I/04	13	MD11I
I/03	11	MD10I
I/02	10	MD09I
I/01	9	MD08I

I82

+12V

24 Vcc

$\overline{CS}$ 18   GND 12

R11 680
R3 10K
C2 .1

CR5

R4 200 1/2W
R5 200 1/2W
R6 200 1/2W

+5V   CR1   CR2   CR6

B1 3.6V

C1 6.8

R7 51

Q1 2N4401-5

R2 22K

R1 4.7K

I5A6   DCOKI

FS-15 POWER DISTRIBUTION

DCOKI 14D4

+5V

RESETRØ 1E3, 11E3, 13B3

J3

DCOKI 5

20

2 MLD9 19
   F244 ŌĒ

10 1

+12V 1
      +12V
      2

+5V 7
     +5V
     8

C12-22   C23-144
47   .1

3

6

9

-12V 4
      -12V

TC640-0781

FS-16 SPARE FUNCTIONS

MLA15 F86 — 13, 12 → 11

MLA15 F86 — 4, 5 → 6

MLB12 F20 — 13, 12, 10, 9 → 8

MLC5 LS374 — 4 2D, 7 3D, 8 4D, 11 CK / 5 2Q, 6 3Q, 9 4Q

902 4MI

MLD9 F244 — 4 1A2, 6 1A3, 11 2AI, 13 2A2, 15 2A3, 17 2A4, 19 2G / 16 1Y2, 14 1Y3, 9 2Y1, 7 2Y2, 5 2Y3, 3 2Y4

MLH2 F00 — 13, 12 → 11

MLH2 F00 — 10, 9 → 8

MLC11 LS02 — 5, 6 → 4

MLC11 LS02 — 8, 9 → 10

MLE1 F02 — 8, 9 → 10

MLE8 LS04 — 1 → 2

MLE8 LS04 — 9 → 8

MLF1 F32 — 4, 5 → 6

MLF1 F32 — 13, 12 → 11

MLF1 F32 — 10, 9 → 8

MLG1 LS08 — 13, 12 → 11

MLH3 LS10 — 1, 2, 13 → 12

MLH3 LS10 — 11, 10, 9 → 8

MLK2 F00 — 13, 12 → 11

MLK3 LS04 — 3 → 4

MLK3 LS04 — 5 → 6

MLK3 LS04 — 11 → 10

TC640-0781

INFORMATION NOTES

101. ALL VOLTAGES ARE DC UNLESS OTHERWISE SPECIFIED.

102. ALL RESISTANCE VALUES IN OHMS AND 1/4 WATT UNLESS OTHERWISE SPECIFIED.

103. ALL CAPACITANCE VALUES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

104. REFER TO 410972 TERMINAL LOGIC CARD ASSEMBLY DRAWING FOR COMPONENT LOCATIONS.

105. SUPPLY VOLTAGES FOR DUAL-IN-LINE INTEGRATED CIRCUIT PACKAGES:

14 PIN

16 PIN

20 PIN

24 PIN

28 PIN

40 PIN

16 PIN

14 PIN

404264
64K X 1 RAMS

335828
LINE DRIVER
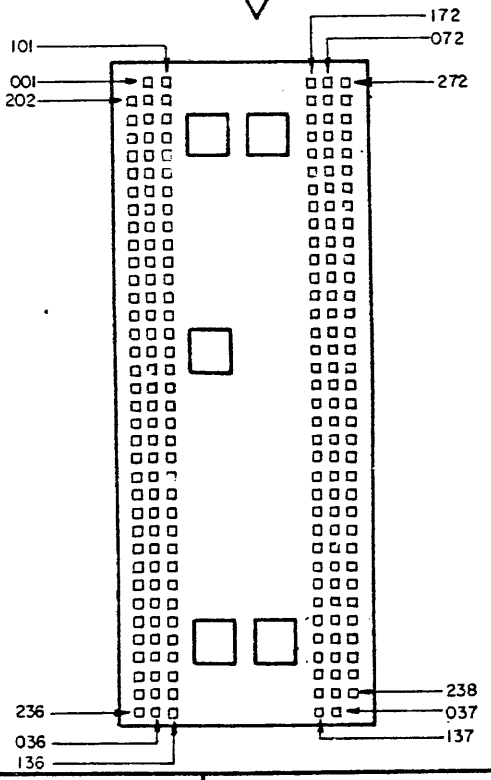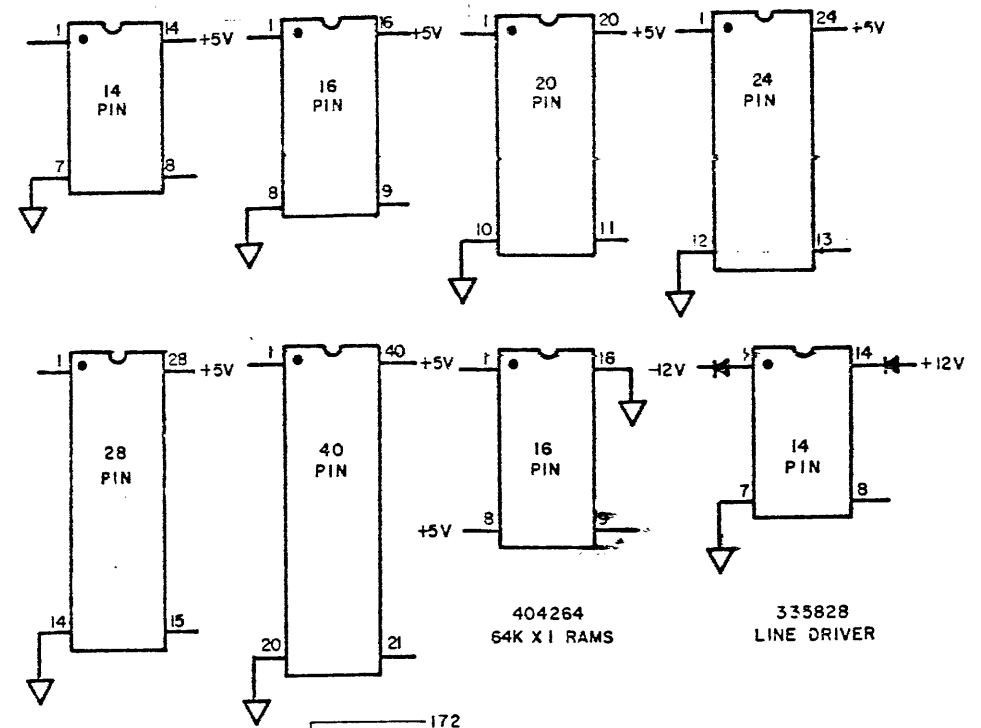
GROUND PINS:

1 , 2 , 3	69, 70, 71
5 , 6 , 7	65, 66, 67
9 , 10, 11	61, 62, 63
13, 14, 15	57, 58, 59
17, 18, 19	53, 54, 55
21, 22, 23	49, 50, 51
25, 26, 27	45, 46, 47
29, 30, 31	41, 42, 43
33, 34, 35	37, 38, 39

+5V PINS

4	72
8	68
12	64
	60
20	56
24	52
28	48
32	44
36	40

106. OPTION STRAPS

STP1

STRAP INSERTED

STRAP REMOVED
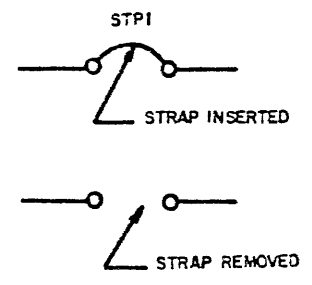
107. SHEET COORDINATE LOCATION LEGEND

5 A 4

— COLUMN ACROSS SHEET BOTTOM
— ROW ALONG SHEET EDGE
— SHEET NUMBER
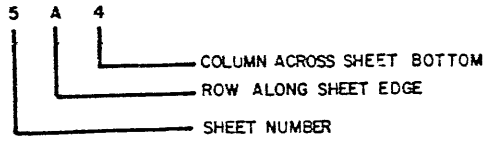
108. CIRCUIT ELEMENT NOTATION

ML	=	INTEGRATED CIRCUIT(S)
OS	=	OPTION SWITCH
RP	=	RESISTOR PACK
CR	=	DIODE
STP	=	STRAP
R	=	RESISTOR
C	=	CAPACITOR
X	=	CRYSTAL OSCILLATOR
Q	=	TRANSISTOR

THE NUMBER OR LETTER-NUMBER AFTER THE ELEMENT NOTATION IDENTIFIES THE SPECIFIC COMPONENT.

109. LOGIC ELEMENT NOTATION

— LOGIC FUNCTION
— DEVICE TYPE
— PIN NUMBER

MLH1
109
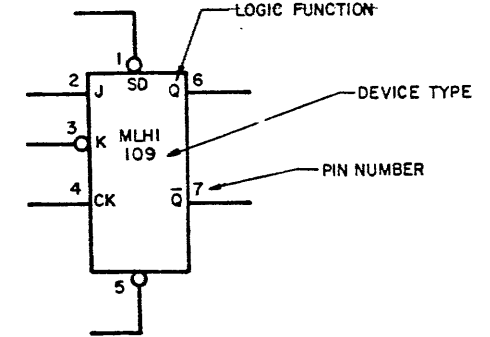
110. CONNECTOR IDENTIFICATION

J2 ← CONNECTOR DESIGNATION
12 ← PIN NUMBER
MALE PIN —

CAN ALSO BE SHOWN AS: J2-12

111. LOGIC BUS NOTATION

A0
A1
A2
A3
A4
A5
A6
A7

AA-NOT CONNECTED TO BUS

BB-CONNECTED TO BUS
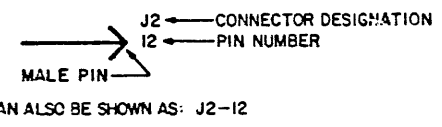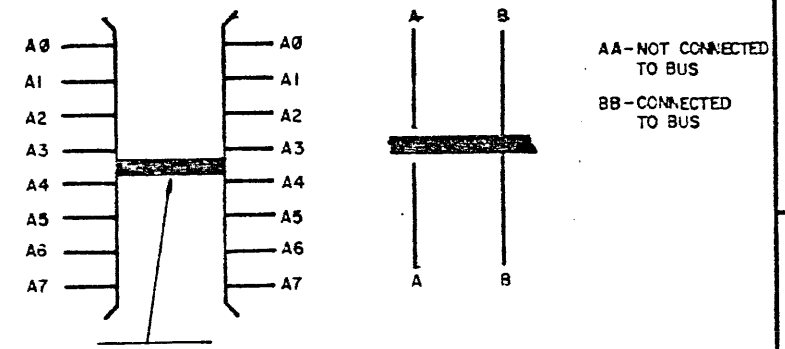
HEAVY LINE INDICATES BUS HAVING A "1 TO 1" RELATIONSHIP OF LEADS ENTERING AND LEAVING.

112. SIGNAL NAMES

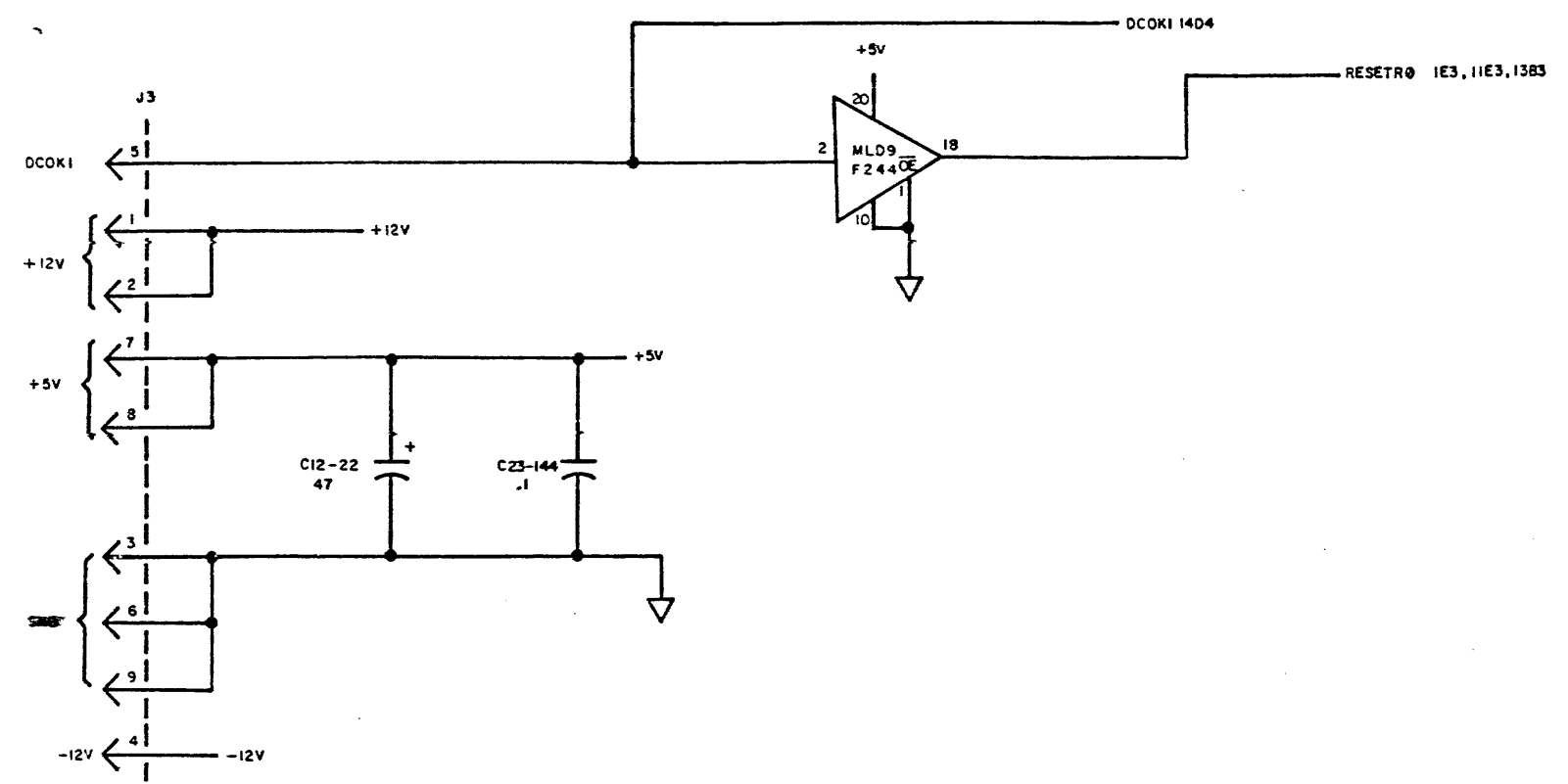THE LAST CHARACTER IN A SIGNAL NAME WILL EITHER BE A "1" OR A "0"; THIS INDICATES THE ACTIVE STATE OF THE SIGNAL 1 = LOGICAL 1 (HIGH); 0=LOGICAL 0 (LOW).
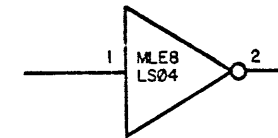
TELETYPE CORPORATION
SKOKIE, ILLINOIS

5620
DOT MAPPED DISPLAY
TERMINAL LOGIC CARD

4972SD-D1

CONNECTOR DEFINITION

201.

J1 PIN ASSIGNMENT

PIN	SYMBOL	DEFINITION	SHEET LOC.
1	HSYNC	HORIZ. SYNC TO MONITOR	
2	VSYNC	VERT. SYNC TO MONITOR	
3	GND	DC GROUND	
4	VIDEO	VIDEO SIGNAL TO MONITOR	
5	NOT USED	NO CONNECTION	
6	GND	DC GROUND	

202.

J2 PIN ASSIGNMENT

PIN	SYMBOL	DEFINITION	SHEET LOC.
1	-12V	-12 VOLTS	
2	MS_IN	SERIAL DATA FROM KEYBOARD	
3	MS_OUT	SERIAL DATA TO KEYBOARD	
4	+5V	+5 VOLTS	
5	GND	DC GROUND	
6	X1	ENCODER OUTPUT FROM MOUSE	
7	X0	ENCODER OUTPUT FROM MOUSE	
8	MB0C0	LEFT BUTTON FROM MOUSE	
9	MB2C0	RIGHT BUTTON FROM MOUSE	
10	MB1C0	CENTER BUTTON FROM MOUSE	
11	Y0	ENCODER OUTPUT FROM MOUSE	
12	+5V	+5 VOLTS	
13	Y1	ENCODER OUTPUT FROM MOUSE	
14	GND	DC GROUND	
15	DTR	DATA TERMINAL READY	
16	+5V	+5 VOLTS	
17	-12V	-12 VOLTS	
18	DSR	DATA SET READY	
19	DCD	DATA CARRIER DETECT	
20	+12V	+12 VOLTS	
21	RD	RECEIVE DATA	
22	SD	SEND DATA	
23	CTS	CLEAR TO SEND	
24	GND	DC GROUND	
25	AUX.DSR	AUXILLIARY DATA SET READY	
26	AUX.SD	AUXILLIARY SEND DATA	
27	PORTEN0	PARALLEL PORT ENABLE	
28	STROBE0	PARALLEL DATA STROBE	
29	+12V	+12 VOLTS	
30	+5V	+5 VOLTS	
31	INT1	INTERRUPT REQUEST	
32	INT0	INTERRUPT REQUEST	
33	PIOD7	PARALLEL INTERFACE BIT 7	
34	-12V	-12 VOLTS	
35	TIME0	PROCESSOR WAIT	
36	ADDR041	PARALLEL INT. ADDRESS BIT 4	
37	PIOD5	PARALLEL INTERFACE BIT 5	
38	PIOD6	PARALLEL INTERFACE BIT 6	
39	ADDR031	PARALLEL INT. ADDRESS BIT 3	
40	ADDR021	PARALLEL INT. ADDRESS BIT 2	
41	PIOD3	PARALLEL INTERFACE BIT 3	
42	PIOD4	PARALLEL INTERFACE BIT 4	
43	ADDR011	PARALLEL INT. ADDRESS BIT 1	
44	ADDR001	PARALLEL INT. ADDRESS BIT 0	
45	PIOD1	PARALLEL INTERFACE BIT 1	
46	PIOD2	PARALLEL INTERFACE BIT 2	
47	PIOWEN0	PARALLEL INT. WRITE ENABLE	
48	PIOEN0	PARALLEL INT. ENABLE	
49	PIORST	PARALLEL INT. RESET	
50	PIOD0	PARALLEL INTERFACE BIT 0	

203.

J3 PIN ASSIGNMENT

PIN	SYMBOL	DEFINITION	SHEET LOC.
1	+12V	+12 VOLTS FROM SUPPLY	
2	+12V	+12 VOLTS FROM SUPPLY	
3	GND	DC GROUND	
4	-12V	-12 VOLTS	
5	DCOKI	+5 VOLTS IS GOOD	
6	GND	DC GROUND	
7	+5V	+5 VOLTS	
8	+5V	+5 VOLTS	
9	GND	DC GROUND	

204. THE 410972 AND 410128 MAY BE EQUIPPED WITH ONE OF
TWO DIFFERENT PROCESSORS:

404132 PROCESSOR:

MLB13-416514 I.C. CLOCK OSCILLATOR 28.8 MHz
MLB15-404132 I.C. BELLMAC 32A

410862 PROCESSOR:

MLB13-NO PART
MLB15-410862 I.C. BELLMAC 32B CPU CARD ASM.

FIRMWARE IN POSITIONS MLG14, MLH14, MLK14, MLL14, MLG15,
MLH15, MLK15, MLL15 MUST BE COMPATIBLE WITH THE
PROCESSOR USED. REFER TO 410972 OR 410128 DRAWING
FOR FIRMWARE COMPATIBILITY.

5620
DOT MAPPED DISPLAY
TERMINAL LOGIC CARD

TELETYPE CORPORATION
SKOKIE, ILLINOIS

4972SD-D2

404132 (32A) PROCESSOR TIMING ***

7.2MHz CYCLES | 4 8 12 16 20 | 4 8 12 16 20 | 4 8 12 16 20

OPERATION | WRITE | READ | INTERRUPT

R1W0
PREVIOUS VALID — ? — CURRENT VALID
PREVIOUS VALID — ? — CURRENT VALID

MA221-MA021
PREVIOUS VALID — ? — CURRENT VALID
? — CURRENT VALID
PREVIOUS VALID — VALID ACKNOWLEDGED INTERRUPT LEVEL

AS0

DS0,WS30-WS00

WSEL00,*CAHIT0**

MD311-MD001
PREVIOUS VALID — DATA VALID — DATA VALID — INTERRUPT VECTOR VALID

XIPL30-XLPL00
PREVIOUS OR NO INTERRUPT PENDING | PREVIOUS OR NO INTERRUPT PENDING | ? | PRIORITY LEVEL OR CURRENT INTERRUPT REQUEST VALID | ? | NEXT OR NO FURTHER INTERRUPT PENDING

IACK0

* DURING A RAM READ OR WRITE OPERATION WSEL00 MAY GO LOW LATER THAN INDICATED CAUSING THE PROCESSOR TO WAIT UNTIL THE RAM IS AVAILABLE. FOR ALL NON-RAM READ AND WRITE OPERATIONS, WSEL00 OR CAHIT0 WILL GO LOW WHEN AS0 IS LOW.

** CAUSES A 16 CYCLE READ OPERATION. CYCLES 12 THROUGH 15 ARE OMITTED FROM THE READ.

*** FOR 410862(32B) PROCESSOR TIMING, REFER TO PAGE E6.

5620
DOT MAPPED DISPLAY
TERMINAL LOGIC CARD

TELETYPE CORPORATION
SKOKIE, ILLINOIS

4972SD-E1

TC640-0781

DYNAMIC RAM TIMING (FS-6 MEMORY ARBITER)

Signal		
32MHz CYCLES		
OPERATION		

PROCESSOR WRITE	DISPLAY READ	PROCESSOR READ

PREQ MLEI-13 — I = PROCESSOR REQUEST RAM

DREQI MLC5-16 — I = DISPLAY REQUEST RAM

PQI MLJ2-1 — I = PROCESSOR HAS RAM

DQI MLJ2-4 — I = DISPLAY HAS RAM

RAS0 MLL2-II — 0 = LOAD ROW ADDRESS

CAS0 MLL3-13 — 0 = LOAD COLUMN ADD & DATA

RAM ADD. PINS — PROW · PCOLUMN · DROW · DCOLUMN · PROW · PCOLUMN — RAM ADDRESS

RAM DATA PINS — IN · OUT · OUT — RAM DATA

RAM WE PINS — 0 = ENABLE WRITE

ENSEL00 MLJ2-13 — 0 = RAM READY FOR PROCESSOR

PLOADI MLJI-10 — I = LOAD PROCESSOR DATA LATCH

DPREQ MLKI-7 — I = LOAD DISPLAY DATA REG.

* THESE SIGNALS CAN BE FOUND ON FS-2 THROUGH FS-5

5620
DOT MAPPED DISPLAY
TERMINAL LOGIC CARD

4972SD-E2

TC640-0781

MOUSE TIMING

X_0, Y_0

X_i, Y_i

$U/\bar{D}$
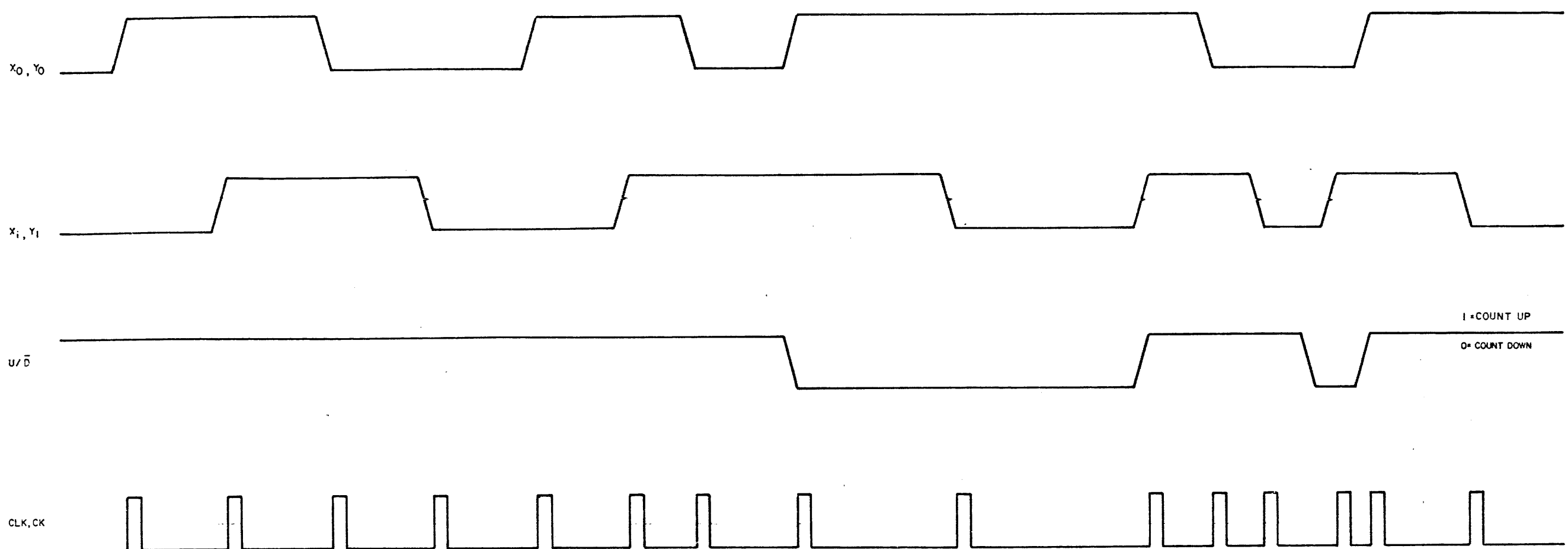
I = COUNT UP

O = COUNT DOWN

CLK, CK

COORDINATE COUNT

| 0 | I | 2 | 3 | 4 | 5 | 6 | 7 | 6 | 5 | 6 | 7 | 8 | 7 | 6 | 5 |

DISPLAY TIMING (FS-7 DISPLAY TIMING & FS-8 DISPLAY ADDRESS)

HORIZONTAL TIMING

4MHz CLOCK CYCLES

MLC4-6 ADDCNT — I = ADDRESS COUNTER ENABLE

RAM ADDRESS TO READ 25 WORDS — RAM ADDRESS FOR DISPLAY READ

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25

NOT VERTICAL BLANK ONLY

MLC4-7 DREQI — I = REQUEST RAM

MLC4-8 VCEI — I = VERTICAL COUNTER ENABLE (MLB4, MLB3, MLA2

MLC4-9 LHCO — O = LOAD HORIZONTAL COUNTER (MLA6, MLA5)

MLC4-11 ADDLOAD — O = LOAD ADDRESS COUNTER (MLE5, MLE4, MLE3, MLE2)

VERTICAL BLANK ONLY

NOT VERTICAL BLANK ONLY

MLC4-12 SRLOAD I — I = LOAD WORD INTO LOW SPEED VIDEO SHIFT REG. (MLF2 TO MLF5)

MLC4-13 SVBI — I = SAMPLE VERTICAL BLANK

MLC4-14 HSYNC — I = HORIZONTAL SYNC MONITOR

HORIZONTAL SCAN CYCLE

HORIZONTAL RETRACE BLANKED | HORIZONTAL TRACE DISPLAYED

64 KHz CLOCK CYCLES

MLC3-6 — O = VERTICAL SYNC MONITOR

MLC3-7 — I = VERTICAL BLANK

VERTICAL TIMING

MLC3-8 LVCO — O = LOAD VERTICAL COUNTER

VIDEO TIMING

FS-9 VIDEO TIMING & SHIFT REGISTERS
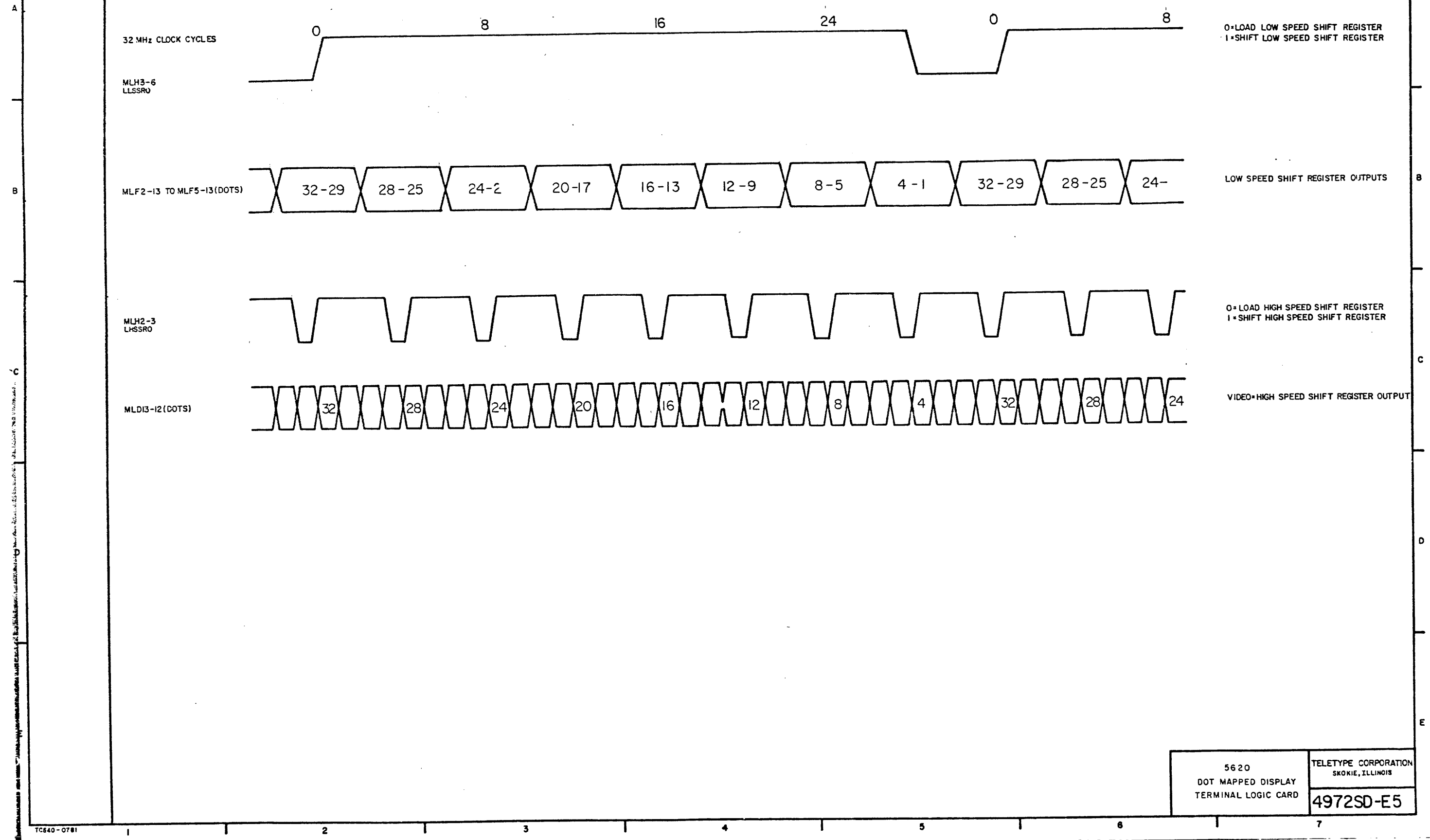
32 MHz CLOCK CYCLES   0   8   16   24   0   8

MLH3-6
LLSSRO
0 = LOAD LOW SPEED SHIFT REGISTER
1 = SHIFT LOW SPEED SHIFT REGISTER

MLF2-13 TO MLF5-13 (DOTS)   32-29 | 28-25 | 24-2 | 20-17 | 16-13 | 12-9 | 8-5 | 4-1 | 32-29 | 28-25 | 24-
LOW SPEED SHIFT REGISTER OUTPUTS

MLH2-3
LHSSRO
0 = LOAD HIGH SPEED SHIFT REGISTER
1 = SHIFT HIGH SPEED SHIFT REGISTER

MLD13-12 (DOTS)   32   28   24   20   16   12   8   4   32   28   24
VIDEO = HIGH SPEED SHIFT REGISTER OUTPUT

410862 (32B) PROCESSOR TIMING

EPROM READ-TWO WAIT STATES

CLK34-ML2-1
AS-ML2-5
EPROM_CE-MLF15-4
EPROM_OE-MLE7-3
PAL_A-ML2-17
PAL_B-ML2-16
DTACK-ML2-19
TRACE MEMORY

WIDE MODE 25ns/
SAMPLE-100ns/div   TIME-X_0=600ns
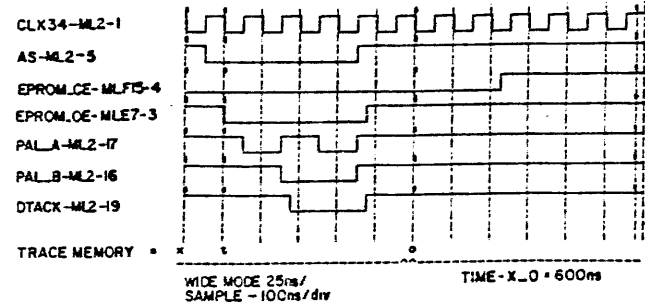
DUART ACCESS-TWO WAIT STATES

CLK34-ML2-1
AS-ML2-5
DUART_CE-MLC12-13
PAL_A-ML2-17
PAL_B-ML2-16
DTACK-ML2-19
TRACE MEMORY

WIDE MODE 25ns/
SAMPLE-100ns/div   TIME-X_0=600ns
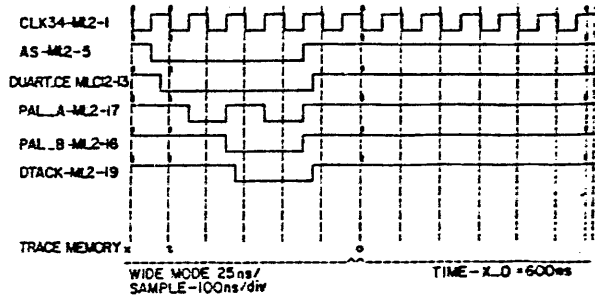
NOTE:
DUART READS AND WRITES ARE EQUIVALENT WITH THE
EXCEPTION THAT DUART WRN (MLA11-8) IS ASSERTED
ON A WRITE AND DUART RDN (MLA11-9) IS ASSERTED
ON A READ.

BRAM READ-ONE WAIT STATE

CLK34-ML2-1
AS-ML2-5
BRAM_OE MLF7-11
PAL_A-ML2-17
PAL_B-ML2-16
DTACK-ML2-19
TRACE MEMORY

WIDE MODE 25ns/
SAMPLE-100ns/div   TIME-X_0=500ns
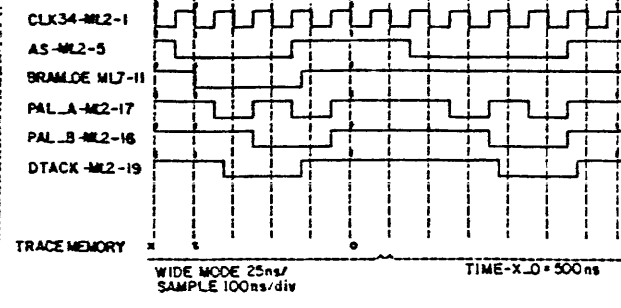
NOTE:
BRAM WRITE IS EQUIVALENT EXCEPT THAT BRAM-WE
(MLE7-8) IS ASSERTED INSTEAD OF BRAM_OE.

ADDCLK WRITE-ZERO WAIT STATE

CLK34-ML2-1
AS-ML2-5
ADDCLK3-MLD2,3,11
PAL_A-ML2-17
PAL_B-ML2-16
DTACK-ML2-19
TRACE MEMORY

WIDE MODE 10/ns
SAMPLE-40ns/div   TIME-X_0=400ns
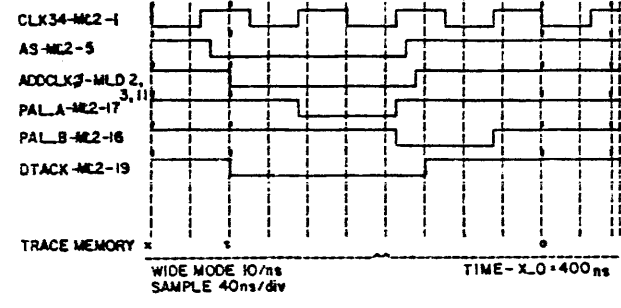
MOUSE READ-ZERO WAIT STATE

CLK34-ML2-1
AS-ML2-5
MOUSE0-MLC12-11
PAL_A-ML2-17
PAL_B-ML2-16
DTACK-ML2-19
TRACE MEMORY

WIDE MODE 10ns/
SAMPLE-40ns/div   TIME-X_0=400ns

RAM READ CYCLE

CLK34-ML2-1
AS-ML2-5
RAM0-MLC12-7
RAS-MLG6-13
CAS-MLG6-14
PLOAD-MLJ1-10
DTACK-ML2-19
TRACE MEMORY

WIDE MODE 25ns/
SAMPLE-100ns/div   TIME-X_0=1ms
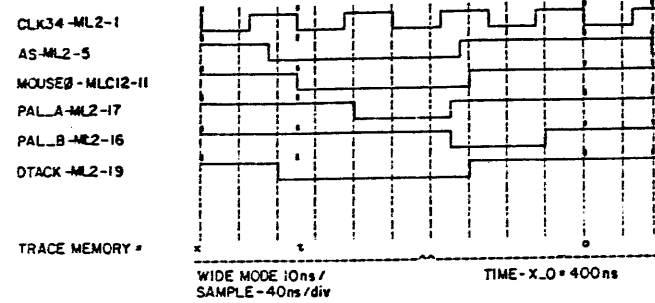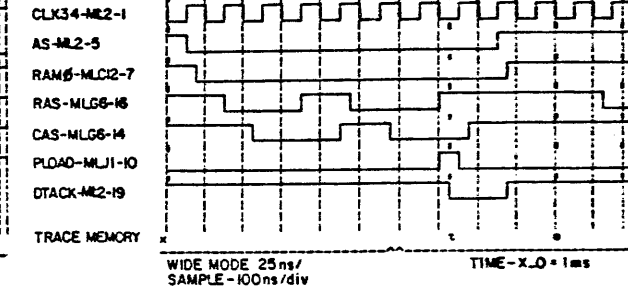
NOTE:
RAM READ CYCLES ARE AT LEAST 600 NSEC (TWO WAIT
STATES) BUT MAY TAKE LONGER DEPENDING ON THE STATE
OF THE MEMORY ARBITER AT THE ASSERTION OF RAM0.

RAM WRITE CYCLE

CLK34-ML2-1
AS-ML2-5
RAM0-MLC12-7
RAS-MLG6-13
CAS-MLG6-14
WRST0-MLF1-3
DTACK-ML2-19
TRACE MEMORY

WIDE MODE 25ns/
SAMPLE-100ns/div   TIME-X_0=800ns
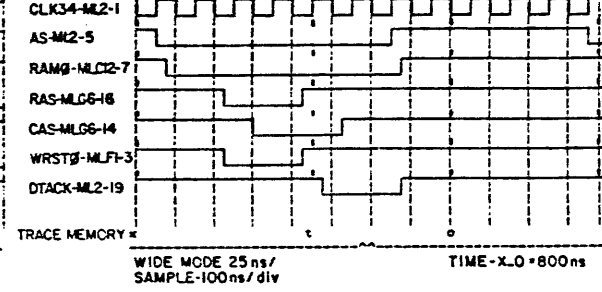
NOTE:
RAM WRITE CYCLES ARE AT LEAST 400 NSEC (ZERO WAIT-
STATE) BUT MAY TAKE LONGER DEPENDING ON THE STATE
OF THE MEMORY ARBITER AT THE ASSERTION OF RAM0.

INTERRUPT ACKNOWLEDGE CYCLE ZERO WAIT STATE

CLK34-ML2-1
AS-ML2-5
PAL_A-ML2-17
PAL_B-ML2-16
IACK-ML2-19
DTACK-ML2-19
TRACE MEMORY

WIDE MODE 10ns
SAMPLE-40ns/div   TIME-X_0=400ns
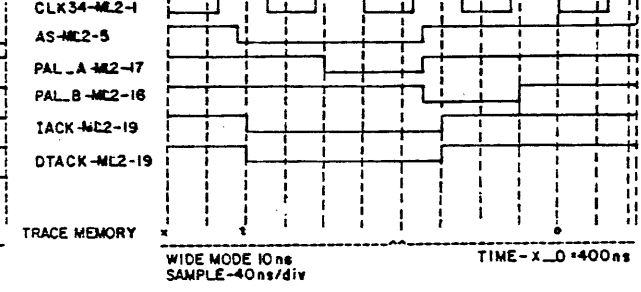
1) TIMING SHOWN IS TYPICAL, AS MEASURED ON A 5620 EQUIPPED WITH A PROTOTYPE 410862 CARD.

2) TIMING DIAGRAMS ARE REFERENCED TO CLK34 STATES (TWO STATES PER CYCLE). EACH CYCLE BEGINS
WITH STATES 0,1,2,3 AND ENDS WITH STATES 4,5,X,X (4,5 AND TWO VESTIGIAL STATES). ADDITIONAL
STATES IN BETWEEN STATES 3 AND 4 ARE WAIT STATES.

3) EACH TRACE SHOWS AN ENTIRE READ, WRITE OR INTERRUPT ACKNOWLEDGE MACHINE CYCLE. THE CYCLE
BEGINS AT THE LEADING EDGE OF CLK34 IN STATE 0 (MARKED X) AND ENDS AT THE TRAILING EDGE OF
THE SECOND VESTIGIAL STATE (MARKED 0). CYCLE DURATION IS INDICATED AT BOTTOM RIGHT CORNER
OF TRACE AS TIME X-0.

4) PAL_A, PAL_B ARE LSB AND SECOND LSB OF PAL COUNTER, RESPECTIVELY. THESE SIGNALS ARE SHOWN
INVERTED ON TIMING DIAGRAMS.

5) IN ALL READ CYCLES, DATA MUST BE SET UP FOR THE CPU 15 ns PRIOR TO THE LEADING EDGE CLK34, STATE 5.

6) IN ALL WRITE CYCLES, DATA IS HELD VALID BY THE CPU TILL THE TRAILING EDGE OF CLK34 IS IN THE
SECOND VESTIGIAL STATE.

7) DTACK MUST BE SET UP 27 ns PRIOR TO A RISING EDGE OF CLK34 TO GUARANTEE RECOGNITION ON THAT EDGE.

TC640-0781

BD-1 BLOCK DIAGRAM

FS-15 POWER DISTRIBUTION
+12V
+5V
-12V
RESETR0

POWER SUPPLY CONNECTOR

FS-2,3,4 & 5 DRAM BYTE 0,1,2,3
RAM DATA OUT
SEL1,D01,PEN0,PLOAD1,RAS00-30,CAS00-30
DISP001-DISP151

MD001-MD311
RWE00-30
MA021-MA191

FS-9 VIDEO TIMING & SHIFT REGISTERS
RVIDEO
VIDEO
SRLOAD1

DREQ1
32M CLOCK

MONITOR CONNECTOR

FS-14 NON VOLATILE MEMORY
MD081-MD151
RIW0
MA021-MA121
BRAM0

FS-12 EPROM AND SELECT LOGIC
MD001-MD311
WS00-30
MA02I AATT,MAZZT
EPROM0

FS-1 BELLMAC 32 PROCESSOR

RIW0 & DS0
WRST0
RAM0
ENSEL00

FS-6 MEMORY ARBITER
DREQ1

MD161-MD311
ADDCLK0

FS-7 & 8 DISPLAY TIMING
VSYNC, HSYNC

DOG CLK1

FS-13 PARALLEL INTERFACE
MD001-MD071
PIO01
PIO00
RIW0
WS30
MA021-MA061
PIO0
TIME0

MD001-MD071
INTKBD
INTM0
INT232R
INT232S
RIW0
MA021-MA051
DUART0

FS-11 KEYBOARD AND EIA INTERFACES

AUX PRINTER EIA RS232C CONNECTOR

LINE EIA RS232C CONNECTOR

KEYBOARD CONNECTOR

PARALLEL PORT CONNECTOR

MD001-MD011
MD161-MD271
MOUSE 0

MOUSE CONNECTOR

FS-10 MOUSE DECODING
MB0, MB1, MB2

TC640-0781

SHEET INDEX AND ISSUE CONTROL	4862 CD

CIRCUIT DESCRIPTION FOR THE 410862 CPU CARD

SHEET 1 OF 1

REVISIONS			SHEET NUMBER									
ISSUE	DATE	AUTH. NO.	1	2	3	4						
1	8-20-84	28702R	1	1	1	1						

SHEET ISSUE NUMBER

APPROVALS			ENG. YB	DSGNR.	DRN. JLO	TELETYPE CORPORATION
PROJ. SUPV.	PROJ.	MFG.REL. COMPL.	DATE 8-20-84	S-NUMBER		SKOKIE, ILLINOIS
		JJK	R&D FILE NO. 3-A185.234A	E-NUMBER		4862 CD

TC-482 (8-81)

CIRCUIT DESCRIPTION FOR THE 410862 CPU CARD

1. INTRODUCTION

The 32B CPU card (TPN 410862) directly replaces the BELLMAC 32A (TPN 404132) microprocessor in the 5620 DMD. It includes the BELLMAC 32B (TPN 352132) microprocessor, the associated clock chip (TPN 416558), and additional emulation circuitry. This emulation circuitry provides wait-state insertion, synthesis of an interrupt acknowledge signal (/IACK)* , and synthesis of byte write strobes. The 32B CPU card emulates only that subset of the 32A functionality which is implemented in the 5620 DMD.

2. MICROPROCESSOR AND CRYSTAL OSCILLATOR

Included on the 32B CPU card are the 32B microprocessor (ML4) and its associated (10 MHz) crystal oscillator chip (ML1). 32B leads which are directly compatible with the 32A are wired directly to the appropriate pins of the 32A footprint. Those which are not directly compatible are wired via the emulation circuitry comprised of ML3 and ML4. Unused 32B inputs are forced to the appropriate logic levels. Unused outputs remain floating.

2.1 32B Architectural Characteristics

Some of the architectural characteristics of the CPU are:

- Sixteen 32-bit registers

- Separate 32-bit address and data busses

- Internal instruction queue and cache

- Extensive pipelining

- Wait-state generation accomodates slow peripherals

See TPN 352132 for more information on the 32B.

---

* In this text, 32B signals which are low true are indicated by a '/' preceeding the signal name. On the accompanying schematics, the same signals are indicated low true by a solid line over the signal name. Recall that 32A signal polarity is indicated by a '0' or '1' suffix. This nomenclature does not apply to the 32B.

2.2 Instruction Set

The 32B supports a powerful instruction set which includes the standard data transfer, arithmetic and logical operations plus unique operations such as modulo math, multiply etc. The large number of program control instructions and operating system instructions make the 32B especially suitable for multi-tasking, UNIX type environments.

The processor's instructions are mnemonic based, assembly language statements. Each instruction is one or two bytes and defines the operation to be performed as well as the operand(s) type. Operands can be bytes, half-words (16-bits), words (32-bits), bit-fields within a word, or blocks and strings of data locations.

2.3 CPU Reads and Writes

Peripheral read and write accesses are at least four cycles of the 10 MHz clock. The CPU begins an access by driving address, data and status onto the appropriate busses. Next, address strobe and data strobe are asserted. The access is not terminated until the peripheral returns a 'ready' signal via /DTACK or /SRDY. Thus, an access can be extended indefinitely to accomodate slow peripherals.

2.4 Faults

Attempts to write to EPROM or 'timeout' are CPU recognized faults. They are reported by an active fault input and terminate bus operations.

2.5 I/O Interrupts

Interrupt requests are acknowledged in an interrupt acknowledge cycle which has the same timing as a read cycle. The interrupt vector is forced onto bits 0 through 7 of the CPU data bus.

2.6 Exceptional Conditions

In addition to interrupt requests and resets, several types of events may interrupt the execution of a program. These events are 'exceptions' and their occurence will cause transfer of program control to the appropriate exception handling routine. When an exception is detected, current process context is stored to allow the process to resume execution once the exception has been handled.

2.7 Pin Assignments

Refer to the 4862SD schematic diagram or TPN 352132 for pin assignments.

2.8 Clock requirements

The two clock inputs to the CPU are driven by oscillator ML1. The oscillator is crystal controlled and provides two 10 MHz signals seperated by 90 degrees of phase.

3. WAIT-STATE INSERTION

The 32B runs at a higher clock frequency than the 32A and requires less clock periods to complete a read or write cycle. This significantly impacts system timing. From timing analysis we see that the emulation hardware will be required to introduce wait-states on peripheral accesses. This is necessary to guarantee that the 32B does not terminate CPU cycles before accessed peripherals are ready.

Two inputs to the 32B (/SRDY and /DTACK) are used to introduce wait-states The CPU will not end a cycle before at least one of these inputs have been asserted. /SRDY is a synchronous input and must not be asserted asynchronously (doing so may cause the CPU to enter a metastable state). Consequently, wait-states are generated using /DTACK exclusively.

The 32B CPU card uses a PAL (ML2) to assert /DTACK. The PAL contains three flip-flops configured as a 3-bit synchronous counter. At the beginning of each machine cycle, when address-strobe (/AS) is high, the counter is loaded with zeros. /AS is subsequently asserted by the CPU, and the counter advances state on each rising edge of CLK34. Thus, the count at any time reflects the number of clock states elapsed in the current machine cycle. The PAL is programmed to assert /DTACK on condition that the required number of wait-states have elapsed (as indicated by the counter) for the accessed peripheral. CPU address leads ADDR20-ADDR22 are provided as PAL inputs and indicate which peripheral is being accessed in each machine cycle. Consider for example an EPROM access, which requires two wait-states. In this case, ADDR20-ADDR22 are all low. The PAL will assert /DTACK when ADDR20-ADDR22 are low, and the counter indicates a count of 2 (two wait-states have elapsed).

From timing analysis the required number of wait-states for each type of access was determined. Note that display RAM and PIO accesses are different from all other accesses in that they are completely asynchronous: The CPU issues a request to access these peripherals at the beginning of a cycle. However, it is not possible to predict how many wait- states will be necessary before the peripherals are ready. In this case, the PAL allows WSEL (generated on the motherboard) to drive /DTACK directly.

Note that the PAL logic equations for /DTACK include a hold term. This term ensures that once /DTACK is asserted, it will be held true until the CPU ends the current cycle (as indicated by negation of /AS).

4. SYNTHESIS OF /IACK

The 32B, unlike the 32A does not provide an explicit interrupt acknowledge. Instead, it provides an interrupt acknowledge cycle status code on status lines SAS0-SAS3. It is necessary to provide an interrupt acknowledge signal (/IACK) when the corresponding code appears on the status lines.

A problem arises in the synthesis of /IACK due to the timing of status codes: The status code for the current cycle remains valid only through state 3. After the trailing edge of state 3, status codes reflect the next cycle status. As a result, it is necessary to 1)hold current cycle status through the end of the current cycle, 2)ensure that status for a following cycle is not interpreted as current cycle status. The PAL will assert /IACK only when the appropriate status code is detected and the counter indicates zero elapsed clock states (i.e. current status valid). A hold term is provided such that /IACK will be held until the interrupt cycle is ended, as indicated by the negation of /AS.

5. SYNTHESIS OF BYTE STROBES

The 32A uses WS00 thru WS30 to enable any subset of the four memory banks corresponding to bytes 0 thru 3. Which of these signals are asserted depends on the type of access: word, upper halfword, lower halfword or any of four bytes. The 32B does not issue seperate enable strobes for each bank. Rather, it provides DSIZE0, DSIZE1, ADDR0 and ADDR1. These output a code corresponding to the type of access. A prom (ML3) is used to generate WS00 thru WS30 from the appropriate permutations of DSIZE0, DSIZE1, ADDR0, ADDR1, /AS and R/W.

3.875

272
Ø72
172

237
Ø37
137

R1   R2   R3   C1   C2   C3

ML2

2.34

C4   C5

ML4

416560 SOCKET

ML3

C6

ML1

A1

C7   C8   C9

1Ø1
ØØ1
2Ø1

136
Ø36
236
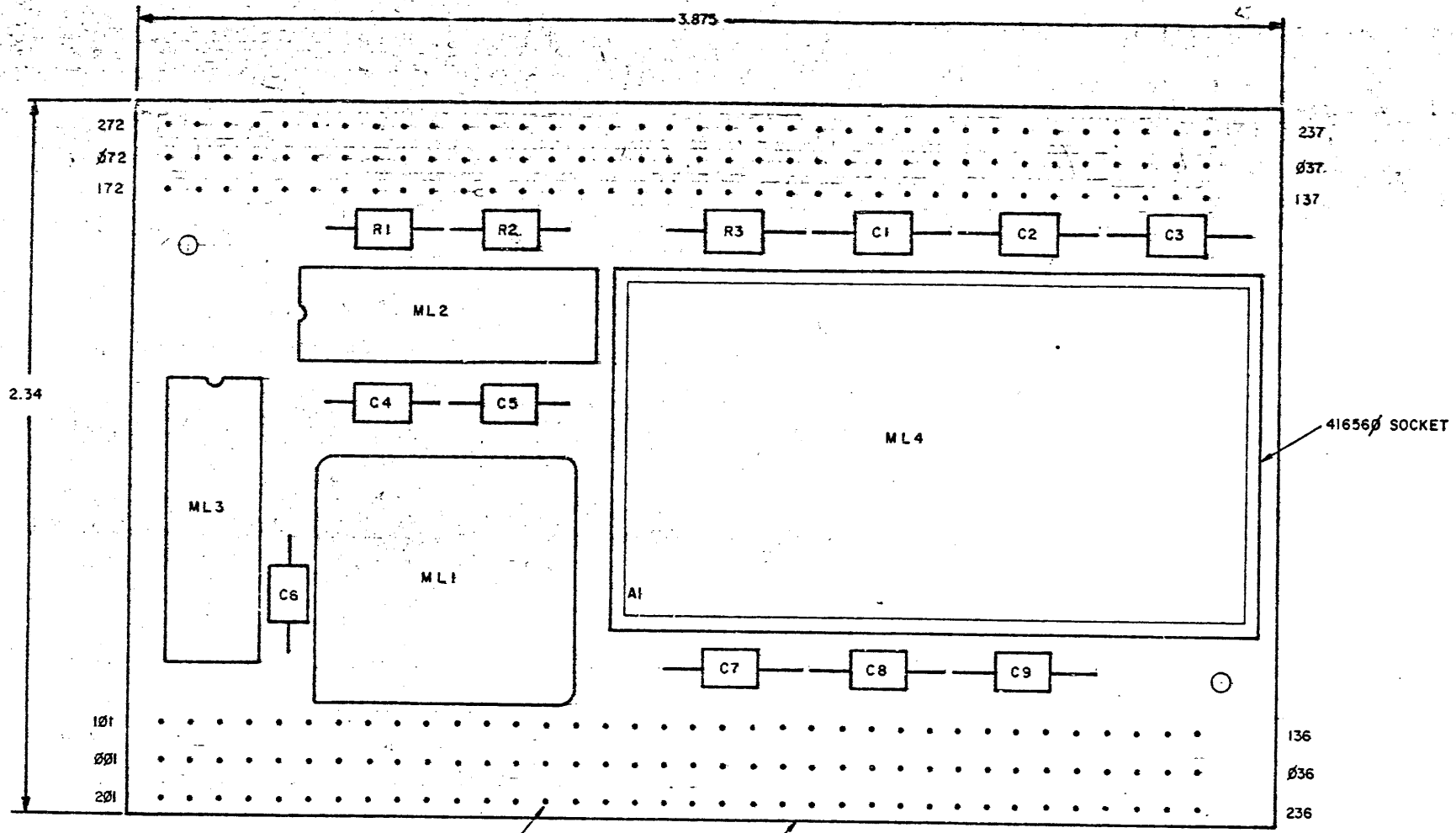
RM NO. 72825
216 SWAGE PINS
.Ø25" DIA. X .225" LONG
PINS EXTEND BELOW
THE BOARD .160" ± .010"
(NON-COMPONENT SIDE)
(32A FOOTPRINT)

409862 ETCHED CIRCUIT BOARD

NOTE: MANUFACTURE PER MR2001

REF. DESIG.	PART NO.	REQ.	DESCRIPTION
ML1	416558		IC, TTL OSC. 10MHZ.
ML2	416557		IC, CPU PAL CODED
ML3	416552		IC, CPU PROM CODED
ML4	352132		IC, CPU 32100
R1-R3	324896		RESISTOR 1.69K 1/8 W
C1-C9	360057		CAPACITOR .01 µF
	72825RN		216 SWAGE PINS
	409862		BOARD, CIRCUIT
	416560		SOCKET, 132 PIN

SIMILAR TO:

REVISIONS

CUSTOMER IDENTIFICATION ISSUE	MFG. VERSION	ASSOCIATED NOTE	DRAWING ISSUE	CONFORMANCE DATE	AUTH. NO.

CIRCUIT CARD

MC

328 CPU
CARD ASSEMBLY

APPROVALS

PROJ. SUPV.	PROJ. DIR.	MFG. REL. COMPL.
ENGR. Y B	DSGNR.	
DRAWN J L O	DATE 4-23-84	
E - NUMBER		
SD - CD NO.		
R & D FILE NO. 3-A185.234A		

TELETYPE CORPORATION

410862 (2 OF 2)

SHEET INDEX

CONTENTS	SHEET NO.	ISSUE NO.																											SHEET NO.
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	
SHEET INDEX	AI	I																												AI
FS-I 328 PROCESSOR	BI	I																												BI
FS-2 POWER DISTRIBUTION	B2	I																												B2
FS-3 FLOATING PINS	B2	I																												B2

SUPPORTING INFORMATION

CATEGORY	NO.
328 CPU CARD ASM	410862
CIRCUIT DESCRIPTION	4862CD

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.

2. THIS SHEET INDEX WILL BE REISSUED AND UPDATED EACH TIME ANY SHEET OF THE DRAWING IS REISSUED OR A NEW SHEET IS ADDED.

3. THE LAST COMPLETED COLUMN INDICATES THE LATEST ISSUE NUMBER OF THE SHEET INDEX.

4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NO.

5. ISSUE DATES WILL BE SHOWN ON THE SHEET INDEX ONLY.

328 CPU CARD

FS-I 32B PROCESSOR

32B CPU CARD

TELETYPE CORPORATION
SKOKIE, ILLINOIS

4862SD-BI

FS-2 POWER DISTRIBUTION

FS-3 FLOATING PINS

(32A FOOTPRINT)

(32B SOCKET)

+5V

GND

C1-C9
.01

+5V

PAL

15	OO
16	A2
17	A1
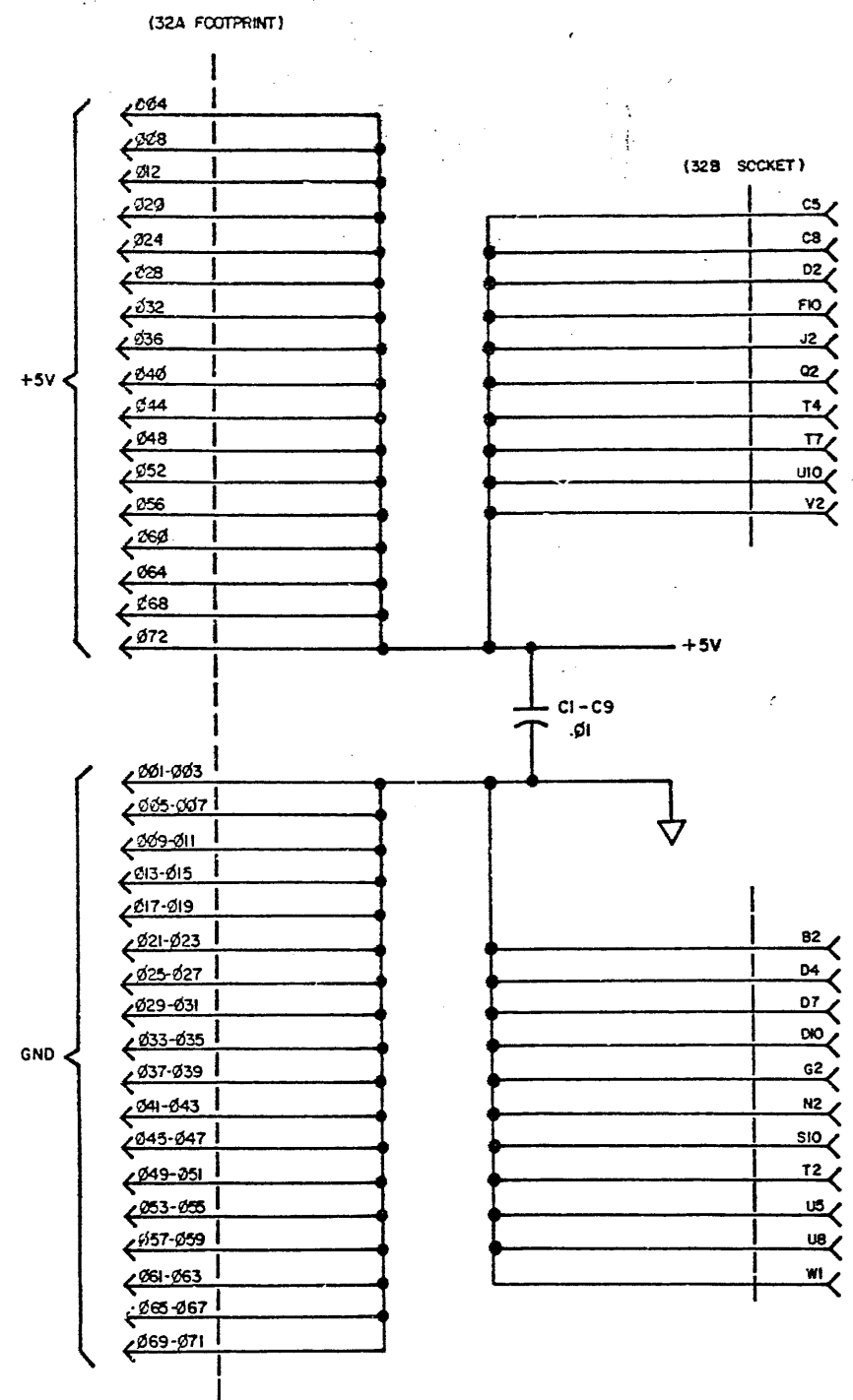
PROM

11	O5
12	O6
13	O7
14	O8

OSC

2	N.C.
4	N.C.
9	N.C.
14	OSC OUT

32A FOOTPRINT

16
102-108
110-112
114-119
123
136-137
141
145
149
153-154
158-165
167-168
170-172
201-203
208
211-220
226
237
240
244
248
252
254-262
265-266
269-272

32B

S1	ADDR24
T1	ADDR25
U1	ADDR26
Q1	ADDR27
P2	ADDR28
R1	ADDR29
R2	ADDR30
S2	ADDR31
U4	IQS0
R5	IQS1
T5	XMD0
S5	XMD1
L11	DRDY
S7	BRACK
V4	SOI

| W8 | RRRACK |

L10	ABORT
Q10	RESET
U11	DO NOT CONNECT
W11	DO NOT CONNECT
W10	DO NOT CONNECT
G11	VAD
K11	DO NOT USE
T11	CYCLE I

32B CPU CARD

TELETYPE CORPORATION
SKOKIE, ILLINOIS

4862SD-B2

TC640-0781

NOTE: MANUFACTURE PER MR2001 AND MR2029 GROUP I

REF. DESIG.	PART NO. REQ.	DESCRIPTION
	409973	BOARD, ETCHED
J105	416504	JACK, 6 POS. MOD.
J104	416505	CONNECTOR, 9 POS. D
J103	416506	CONNECTOR, 25 POS. D
J102	416507	CONNECTOR, 25 POS. D
J101	407721	CONNECTOR
	416503	ASSEMBLY, CABLE
C1-C14	325034	CAPACITOR, 120pf
C16	325034	CAPACITOR, 120pf
C19-C51	325034	CAPACITOR, 120pf
L1-L28	416508	BEAD, FERRITE
L31-L32	416508	BEAD, FERRITE
L37-L102	416508	BEAD, FERRITE
	430756	POST
	110743	WASHER
	151880	NUT
F1-F4	418274	AXIAL PCB FUSE, 5A

430756 POST
110743 WASHER
151880 NUT
(6 PLS)

416506 CONNECTOR

416507 CONNECTOR

J103

J102

410973 ISS.

416505 CONNECTOR

J105   J104

416504 CONNECTOR

418274 AXIAL PCB
FUSE, 5A (4-PLS)

J101

407721 CONNECTOR

325034 CAP
(48 PLS)

416508
FERRITE BEAD
(96 PLS)

409973 BOARD, ETCHED

416503 CABLE ASM.
(SOLDER TO NON-COMP SIDE)

CONNECTOR   POST

COMPONENT SIDE

WASHER   NUT

SIDEVIEW

CONTACT OPENINGS
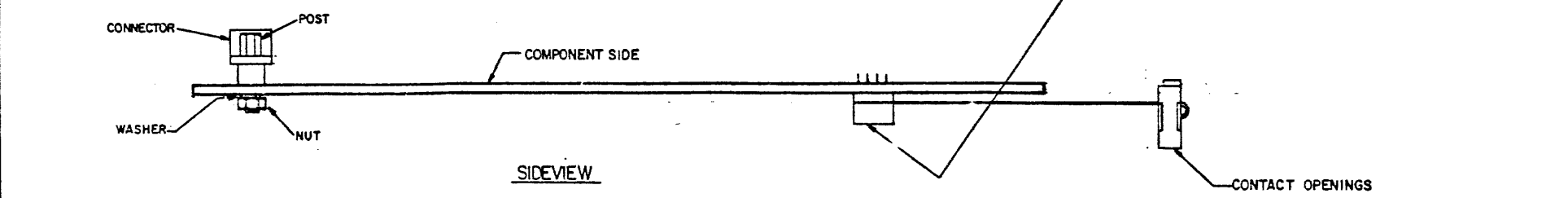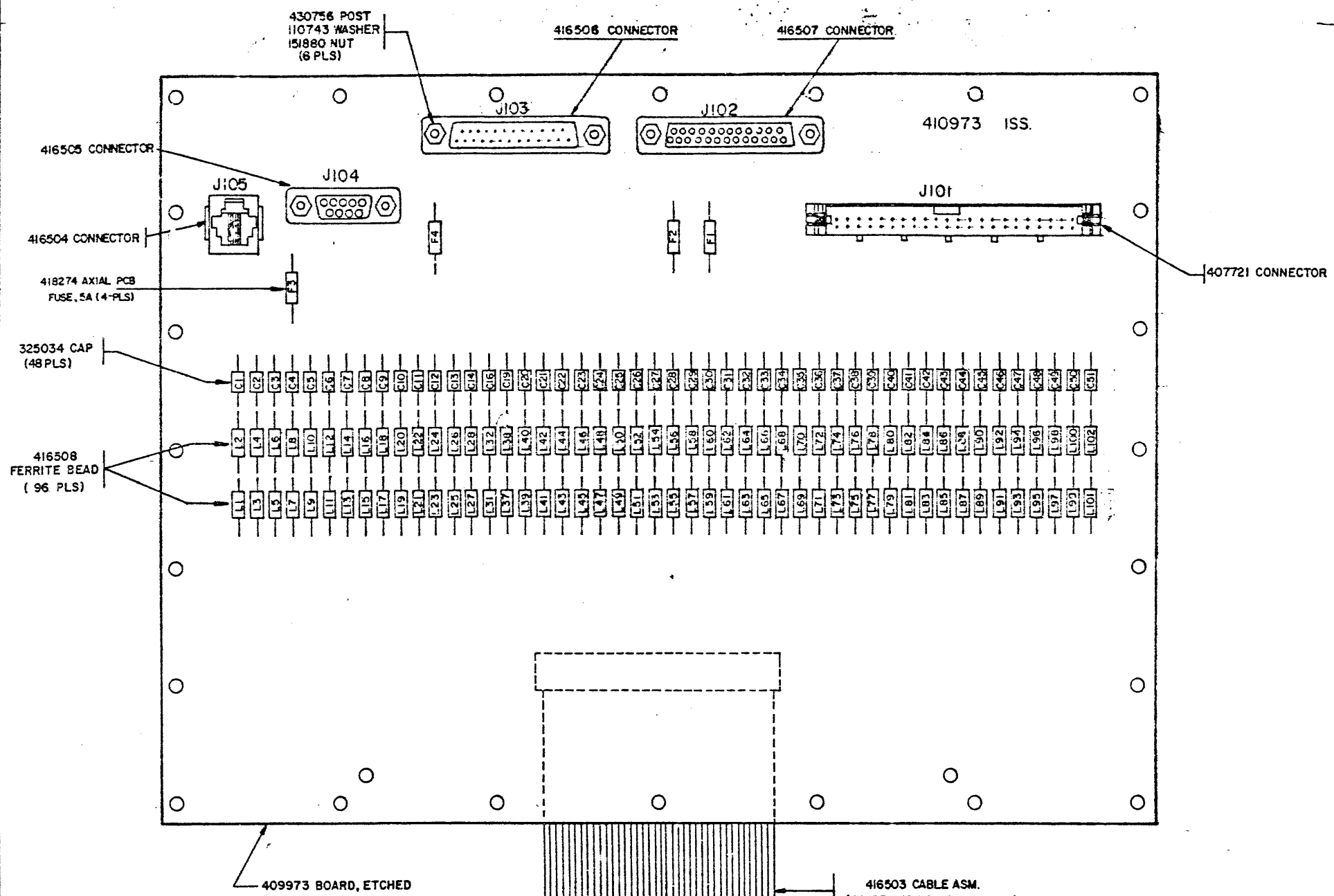
F1-F4 WERE ADDED AT ASSEMBLY ISSUE 3A. L29,L30,L33,L34,L35,
L36,C15,C17 AND C18 WERE ELIMINATED AT ASSEMBLY ISSUE 3A.

SIMILAR TO:

TC637-1060

0

SHEET INDEX

CONTENTS	SHEET NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	SHEET NO.
										ISSUE NO.																
SHEET INDEX	AI	1	2	3																							AI
FS-I — I/O FILTER CARD	BI	1	2	3																							BI

SUPPORTING INFORMATION

CATEGORY	NO.

USE OF SHEET INDEX

WHEN CHANGES ARE MADE IN THIS DRAWING:

1. ONLY CHANGED SHEETS WILL BE REISSUED. (INCLUDING SHEET 1)

2. UNCHANGED SHEETS RETAIN EXISTING ISSUE NUMBER.

THE LAST COMPLETED COLUMN OF THE SHEET INDEX INDICATES THE LATEST ISSUE PER SHEET.

HISTORY NOTES

101. JIO3 PIN 4 CONNECTED TO JIO3 PIN 20 AT ASSEMBLY ISSUE 2. THIS PROVIDES CONTROL OF THE RTS SIGNAL VIA THE DTR SIGNAL.

102. AT ASSEMBLY ISSUE 3A, IT IS NO LONGER NECESSARY TO GREEN WIRE THE CONNECTION FROM JIO3 PIN 4 TO JIO3 PIN 20 AS MENTIONED IN HISTORY NOTE 101. THAT CONNECTION HAS BEEN INCORPORATED INTO THE NEW 409973 ARTWORK.

103. THE FOLLOWING FILTER NETWORKS IN THE EIA I/O - JIO3 CONNECTOR WERE REMOVED AT ASSEMBLY ISSUE 3A.

```
P2                                        JIO3
  20 >——[ L35  L36  C18 ]——> 9      +12VDC

  17 >——[ L33  L34  C17 ]——>10      -12VDC

  16 >——[ L29  L30  C15 ]——>14      +5VDC
```
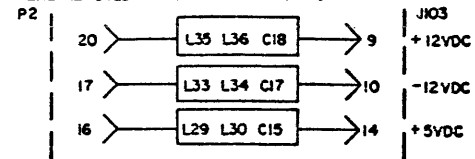
104. FUSES F1-F4 WERE ADDED AT ASSEMBLY ISSUE 3A, FERRITE BEADS L29, L30, L33, L34, L35, L36 AND CAPACITORS C15, C17 AND C18 WERE ELIMINATED AT ASSEMBLY ISSUE 3A.

410973
I/O FILTER CARD

APPROVALS

PROJ. COPY	PROJ. DIV.	MFG. REL. COMPL.

ENGR. ARB   DSGNR. ARB
DRN. JJ T   DATE 6-23-83
R & D FILE 3-AI85.234A
S-NUMBER

TELETYPE CORPORATION

4973SD-AI

TC654-0679

I/O FILTER CARD

PARALLEL I/O

P2   J101

P2	Filter	J101	Signal
28	L99 L100 C50	2	STROBE0
31	L97 L98 C49	4	INT1
32	L95 L96 C48	6	INT0
35	L93 L94 C47	8	TIME
36	L91 L92 C46	10	ADDR041
39	L89 L90 C45	12	ADDR031
40	L87 L88 C44	14	ADDR021
43	L85 L86 C43	16	ADDR011
44	L83 L84 C42	18	ADDR001
47	L81 L82 C41	20	PIOWEN0
48	L79 L80 C40	22	PIOEN0
49	L77 L78 C39	24	PIORST0
50	L75 L76 C38	26	PIOD01
45	L73 L74 C37	28	PIOD11
46	L71 L72 C36	30	PIOD21
41	L69 L70 C35	32	PIOD31
42	L67 L68 C34	34	PIOD41
37	L65 L66 C33	36	PIOD51
38	L63 L64 C32	38	PIOD61
33	L61 L62 C31	40	PIOD71
34	L59 L60 C30	42	-12VDC
29	L57 L58 C29 418274,5A F1	44	+12VDC
		46	+12VDC
30	L55 L56 C28 418274,5A F2	48	+5VDC
		50	+5VDC
27	L53 L54 C27	49	PORT ENABLE0

KEYBOARD I/O

P2   J105

P2	Filter	J105	Signal
2	L5 L6 C3	1	MS/
3	L7 L8 C4	2	MS/OUT
1	L3 L4 C2	3	-12VDC
4	L9 L10 C5 418274,5A F3	4	+5 VDC
		6	FRAME

EIA I/O

P2   J103

P2	Filter	J103	Signal
		1	FRAME
22	L47 L48 C24	2	SD
21	L45 L46 C23	3	RD
23	L43 L44 C22	5	CTS
18	L41 L42 C21	6	DSR
19	L37 L38 C19	8	DCD
15	L31 L32 C16	20	DTR
		4	RTS

SEE HISTORY NOTE #101

AUX. EIA I/O

P2   J102

P2	Filter	J102	Signal
		1	FRAME
26	L49 L50 C25	3	AUX. SD
25	L51 L52 C26	6	AUX. DSR.

MOUSE I/O

P2   J104

P2	Filter	J104	Signal
12	L23 L24 C12 418274,5A F4	1	+5VDC
13	L25 L26 C13	2	Y1
11	L27 L28 C14	3	Y0
6	L11 L12 C6	4	X1
7	L13 L14 C7	5	X0
10	L19 L20 C10	7	MB1C
9	L17 L18 C9	8	MB2C
8	L15 L16 C8	9	MB0C

DC GROUND DISTRIBUTION

P2	Filter	J	
5	L1 L2 C1	J105	5
14	L21 L22 C11	J104	6
24	L39 L40 C20	J103	7
	L101 L102 C51	J101	1-47 (ODD)
		J102	7

TYPICAL NETWORK

INPUT — L_x^* — L_x^* — OUTPUT

C_x 120 pf

FRAME

* ALL OF THE INDUCTIVE FILTERS (L1-L102) ARE FERRITE BEADS MOUNTED TO WIRE LEADS. THE IMPEDANCE OF EACH OF THESE FERRITE BEADS WILL BE:

@ DC (0Hz) = 0 Ω
@ 10 MHz = 39 Ω min.
@ 100 MHz = 80 Ω min.

ISSUE 1 2 3

410973
I/O FILTER CARD

TELETYPE CORPORATION
SKOKIE, ILLINOIS

4973SD-B1

TC640-0731

SHEET INDEX

CONTENTS	SHEET NO.	ISSUE NO. 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	SHEET NO.
SHEET INDEX	AI	1	2	3																								AI
ACTUAL WIRING (USA) —	BI	1	2	3																								BI
COMPONENT LOCATION AND CABLE ROUTING (USA)	B2	1	2	3																								B2
ACTUAL WIRING (OLIVETTI)	B3	—	—	1																								B3
COMPONENT LOCATION AND CABLE ROUTING (OLIVETTI)	B4	—	—	1																								B4

SUPPORTING INFORMATION

CATEGORY	NO.

USE OF SHEET INDEX

WHEN CHANGES ARE MADE IN THIS DRAWING:

1. ONLY CHANGED SHEETS WILL BE REISSUED. (INCLUDING SHEET 1)

2. UNCHANGED SHEETS RE-TAIN EXISTING ISSUE NUMBER.

THE LAST COMPLETED COLUMN ON THE SHEET INDEX INDI-CATES THE LATEST ISSUE PER SHEET.

REVISIONS

ISSUE	DATE	AUTH. NO.
1	8-2-83	29057R
2	11-23-83	27541
3	9-5-84	28110

HISTORY NOTES

1) ISSUE 2 ADDED ACTUAL AND SCHEMATIC VIEWS OF 117366 AND 307544 GROUNDING STRAPS.

ACTUAL
WIRING DIAGRAM
FOR
MODEL 56D502AAA
DOT MAPPED DISPLAY

APPROVALS

PROJ. SUPV	PROJ. DIR	MFG. REL. COMPL.

ENGR. ARB DSGNR. ARB
DRN. JJT DATE 6-23-83
R & D FILE 3-A185.234A
S-NUMBER 62719S

TELETYPE CORPORATION

9671WD-AI

ACTUAL WIRING (USA)

TO MOUNTING STUD ON FAN
307544
TO FAN FRAME
307544
TO MOUNTING STUD ON PEDESTAL
TO MONITOR FRAME
117366

416501

414473
FILTER

410972 TERMINAL LOGIC CARD
OR
410128 TERMINAL LOGIC CARD (XRAM)

410973 I/O FILTER CARD

407088
SWITCH

BLACK
BLACK
BLACK

BLACK
GREEN

WHITE
WHITE
WHITE

J101 — PARALLEL I/O

J102 — AUX. EIA I/O

WHITE   BLACK

414092
POWER SUPPLY

416502   J2   P2

(1)
(3)
(5)

(1)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
(13)

WHITE
ORANGE
ORANGE
RED
RED

BLACK
BLUE
BLACK
BLACK

J3

J103 — EIA I/O

413460
MONITOR

J104 — MOUSE I/O

408980
FAN

WHITE   BLACK

PART OF 413460
MONITOR

J1

J105 — KEYBOARD I/O

(1)   (4)   (4)   (1)

TC 434 (3-69)

REAR VIEW

COMPONENT LOCATION AND
CABLE ROUTING
(USA)

BOTTOM VIEW

413460 MONITOR

414092 POWER SUPPLY

408980 FAN

PART OF 416501 CABLE ASM.
(AC POWER TO MONITOR)

GREEN WIRE FROM
LINE FILTER

BRIGHTNESS CONTROL

407088 SWITCH

BLACK

117366 STRAP

WHITE

BLACK WIRES PART OF 416501 CABLE

414473 LINE FILTER

307544(2) AND 117366 STRAPS
TO PAN STUD, FAN & MONITOR

401582
NUT W/LW

307544
STRAP, GROUNDING (2)

TO FAN

TO LOWER ENCL.

117366 STRAP

TO MONITOR

BLACK & WHITE WIRES ARE
PART OF 416501 CABLE ASM.
(AC POWER TO FAN)

92527
STARWASHER
(4)

PART OF 416501
CABLE ASM.

401582
NUT W/LW

307544 STRAPS FOR
PAN STUD & FAN FRAME

412394 AC CORD

BLACK

WHITE

P1

J2

BRIGHTNESS CONTROL CABLE,
PART OF 413460 MONITOR

J1

410972 TERMINAL LOGIC CARD
OR
410128 TERMINAL LOGIC CARD (XRAM)

J3

PART OF 416501 CABLE ASM.
(AC POWER TO SUPPLY)

416502 CABLE ASM.

410973 I/O FILTER CARD

ACTUAL WIRING
DIAGRAM FOR THE
560502AAA
DOT MAPPED DISPLAY

TELETYPE CORPORATION
SKOKIE, ILLINOIS

9671WD-B2

TC640-0781

ACTUAL WIRING (OLIVETTI)

TO MOUNTING STUD ON FAN

TO FAN FRAME

TO MONITOR FRAME

416556 (3 PLS)

416582

GROUND STUD ON HOUSING PEDESTAL

414473 FILTER

BLUE 0.33 MF BROWN

416561

416553 CABLE ASM. AC

455605 SWITCH

410972 TERMINAL LOGIC CARD
OR
410128 TERMINAL LOGIC CARD (XRAM)

410973 I/O FILTER CARD

BL

BR

414092
POWER SUPPLY

416502

J2

P2

J3

PARALLEL I/O
J101

AUX. EIA I/O
J102

EIA I/O
J103

MOUSE I/O
J104

KEYBOARD I/O
J105

WHITE
ORANGE
ORANGE
RED
RED
BLACK
BLUE
BLACK
BLACK

(1)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
(10)

(5)
(3)
(1)

413460
MONITOR

BL BR

416554
FAN

PART OF 413460
MONITOR

J1

(1) (4)

(4) (1)

REAR VIEW

COMPONENT LOCATION AND
CABLE ROUTING
(OLIVETTI)

BOTTOM VIEW

ISSUE

413460 MONITOR

PART OF 416553 CABLE ASM.
(AC POWER TO MONITOR)

BRIGHTNESS CONTROL

455605 SWITCH

MONITOR LABEL

BLACK

416556 STRAP

WHITE

BROWN & BLUE WIRES ARE
PART OF 416553 CABLE ASM.
(AC POWER TO FAN)

416556 STRAPS FOR
PAN STUD & FAN FRAME

414492 POWER SUPPLY

416554 FAN

G/Y WIRE FROM
LINE FILTER

BLACK WIRES PART OF 416553 CABLE

414473 LINE FILTER W/416561 CAPACITOR
(0.33 MF)

401582
NUT W/LW

416556
STRAP, GROUNDING (2)

416556 GROUND STRAP

92527
STARWASHER
(4)

401582
NUT W/LW

307544 (2) AND 117366 STRAPS
TO PAN STUD, FAN & MONITOR

TO FAN

TO LOWER ENCL.

TO MONITOR

TO 414473 FILTER

416562 STRAP, GROUND

AC CORD

BLACK

WHITE

P1

J2

J1

J3

BRIGHTNESS CONTROL CABLE,
PART OF 413460 MONITOR

410972 TERMINAL LOGIC CARD
OR
410128 TERMINAL LOGIC CARD (XRAM)

PART OF 416553 CABLE ASM.
(AC POWER TO SUPPLY)

416502 CABLE ASM.

410973 I/O FILTER CARD

ACTUAL WIRING
DIAGRAM FOR THE
56D502CAA
DOT MAPPED DISPLAY

TELETYPE CORPORATION
SKOKIE, ILLINOIS

9671WD-B4

TC640-0781

UNIT SET CODE	① COMBINED I.D. PLATE							② NAME PLATE	③ CAUTION PLATE		CUSTOMER MARKING CODE
	LABEL PART NO.	MODEL	SET CODE	SERIAL NO.	CURRENT RATING (AMP)	CANADIAN REG. MARK	VOLTAGE & FREQ. RATING				
56D502AAA	456644	5620AAAI0I	(TYPE)	(TYPE)	1.5		120VAC 50/60Hz	416568	414129		TA
" ABA	"	ABA			"			"	"		"
" BAA	"	BAA			"			416567	"		BI
" BBA	"	BBA			"			"	"		"
" CAA	430587	CAA			0.8		220V 50-60Hz	416564	"		ER
" CBA	"	CBA			"		"	"	"		"

— 430587 LABEL

TELETYPE CORPORATION, SKOKIE, ILLINOIS, USA

CODE

MARCA REGISTRADA

SERIAL NO.

220V 50-60Hz 0.8A
FABRIQUE EN USA
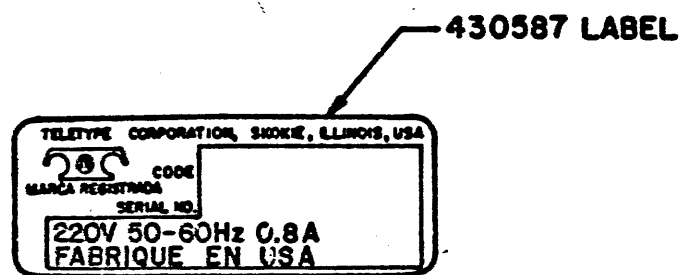
NOTE: TYPE IN INFORMATION AS SHOWN, IN ADDITION TO CODE AND SERIAL NO.

5620

±.031
.281

②

FRONT VIEW

±.094
.1875

±.094
.125

WARNING

③ ①

REAR VIEW

1.000 ±.031
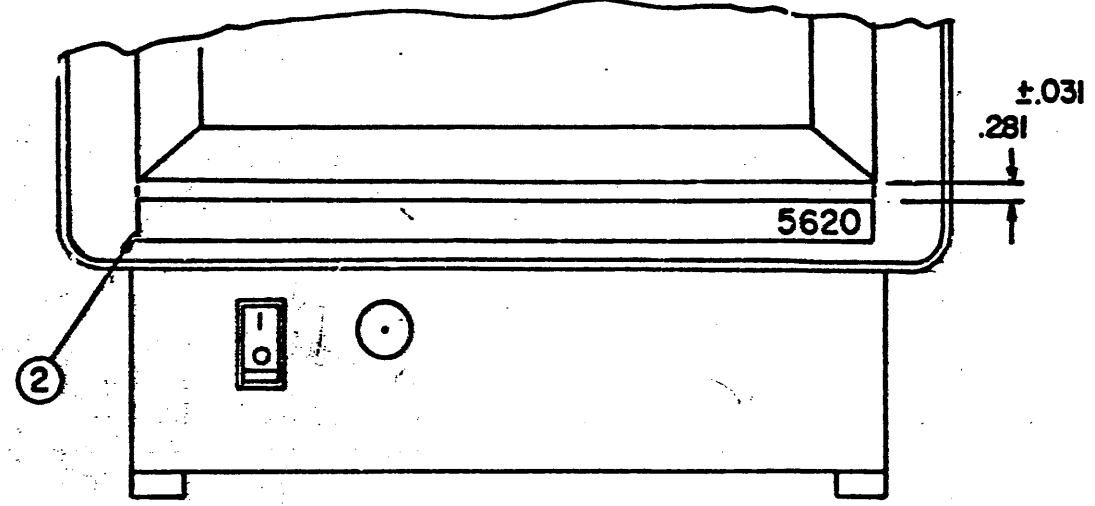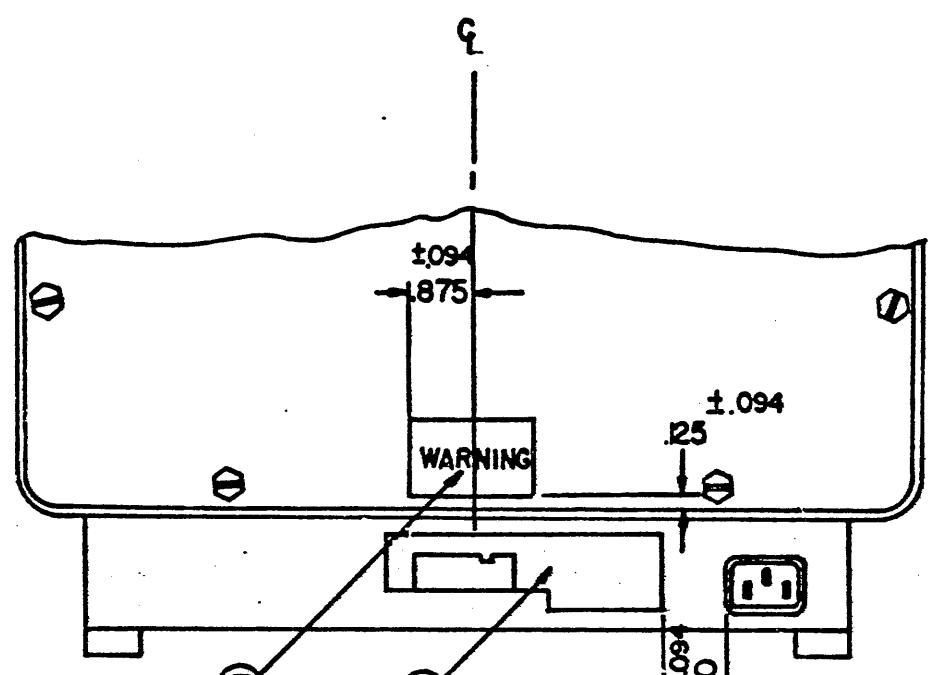
MARKING CHART
FOR
MODEL 56D502
DISPLAY
MODULE

APPROVALS

PROJ. SUPV.	PROJ. BTR.	MFG. REL. COMPL.

ENGR. KS | DSGNR.
DRN. JLO | DATE 6-14-84
R & D FILE 3-A185.234A
S-NUMBER

TELETYPE CORPORATION

56D502/MC

TC256-0879

AT&T
5620
Motorola
Monitor
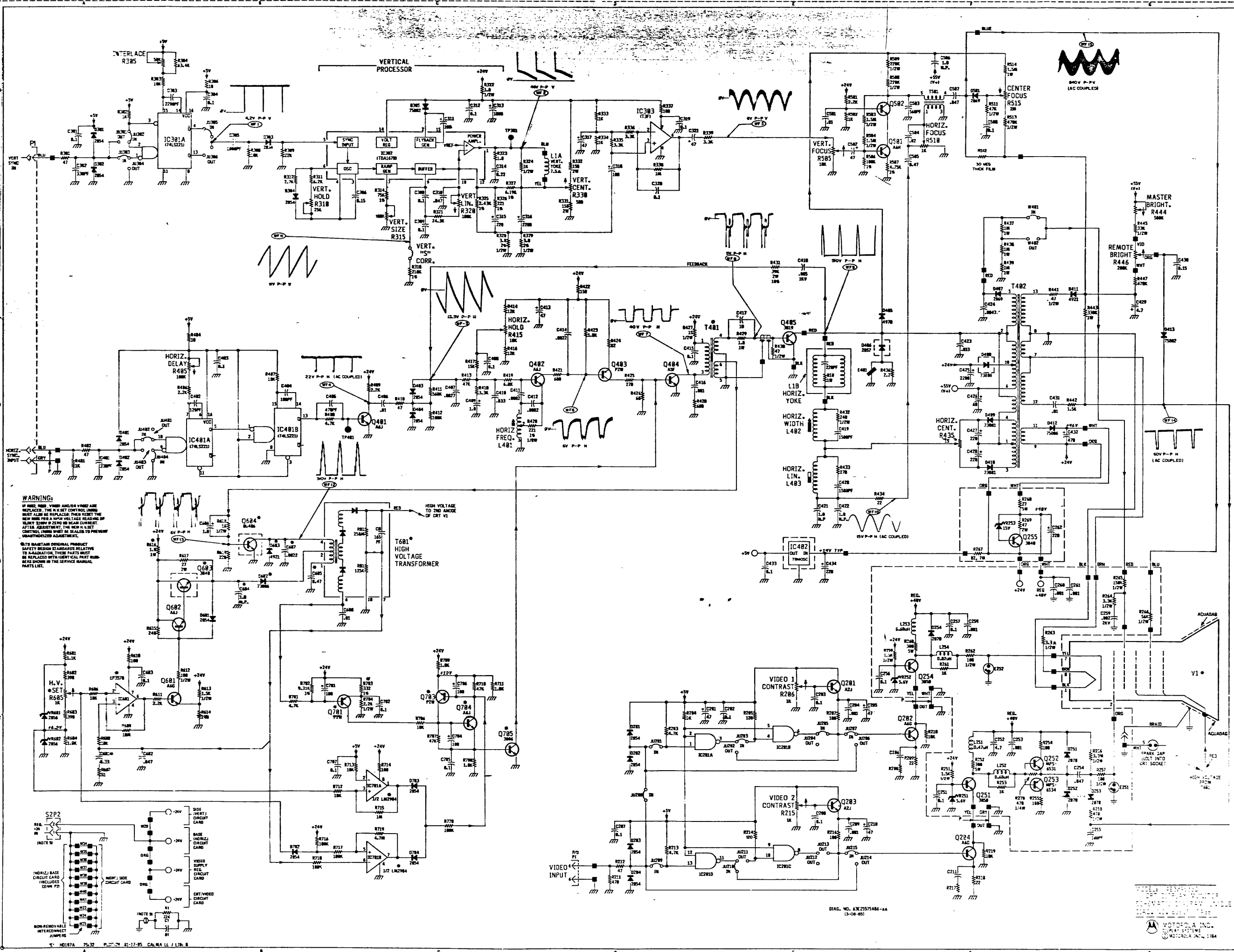
5620
Ball Monitor
1 of 6

VERTICAL DRIVE WAVEFORMS ARE WITH HORIZONTAL OUTPUT TRANSISTORS Q1, Q2 DISABLED BY DISCONNECTING J101.

VERT: 1V/DIV	VERT: 2V/DIV	VERT: 2V/DIV	VERT: 5V/DIV	VERT: 5V/DIV	VERT: 10V/DIV	VERT: 2V/DIV	VERT: 20V/DIV	VERT: 5V/DIV	VERT: 20V/DIV
HORIZ: 2mS/DIV	HORIZ: 2mS/DIV	HORIZ: 2mS/DIV	HORIZ: 2mS/DIV	HORIZ: 2mS/DIV	HORIZ: 2mS/DIV	HORIZ: 2mS/DIV	HORIZ: 2 mS/DIV	HORIZ: 2mS/DIV	HORIZ: 2mS/DIV
VDC: 3.7	VDC: 2.3	VDC: 4.2	VDC: 13.5	VDC: 70.3	VDC: 9.3	VDC: 4.7	VDC: 65.8	VDC: 34.9	VDC: 34.1
TP115	TP116	TP118	TP117	TP119	TP120	TP122	TP121	TP124	TP123

VERTICAL DRIVE TEST POINTS

LAST FOUR DIGITS OF PWA NO. → XXXX-XX
REVISION LEVEL IDENTIFIER → XXXX-XX

CRT BIAS CIRCUITS TEST POINTS

TP125 VERT: 2V/DIV HORIZ: 2mS/DIV VDC: 4.2
TP126 VERT: 50V/DIV HORIZ: 2mS/DIV VDC: 110
TP114 +716 VDC
TP113 +359 VDC
TP127 VERT: 100V/DIV HORIZ: 5µS/DIV VDC: 0
TP112 VERT: 50V/DIV HORIZ: 5µS/DIV VDC: 424
TP107 VERT: 2V/DIV HORIZ: 10µS/DIV VDC: 4.9

HORIZONTAL DRIVE TEST POINTS

TP110	TP109	TP102	TP101-2	TP103	TP104	TP108	TP111	TP106	TP105
VERT: 5V/DIV	VERT: 50V/DIV	VERT: 2V/DIV	VERT: 2V/DIV	VERT: 2V/DIV	VERT: 2V/DIV	VERT: 2V/DIV	VERT: 50V/DIV	VERT: 2V/DIV	VERT: 2V/DIV
HORIZ: 10µS/DIV	HORIZ: 10µS/DIV	HORIZ: 10µS/DIV	HORIZ: 10µS/DIV	HORIZ: 10µS/DIV	HORIZ: 10µS/DIV	HORIZ: 10µS/DIV	HORIZ: 5µS/DIV	HORIZ: 10µS/DIV	HORIZ: 10µS/DIV
VDC: -0.8	VDC: 63.7	VDC: 8.8	VDC: 2.0	VDC: 4.0	VDC:5.2	VDC: 2.2	VDC: 68.8	VDC: 10.9	VDC: 6.3

TP101-1 VERT: 2V/DIV HORIZ: 10µS/DIV VDC: 2.6

4-12
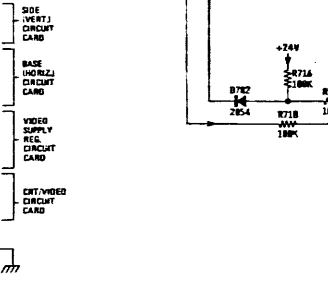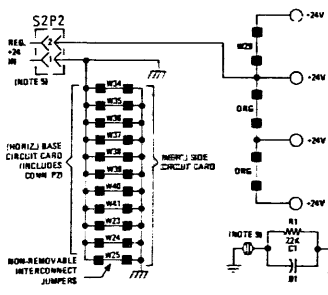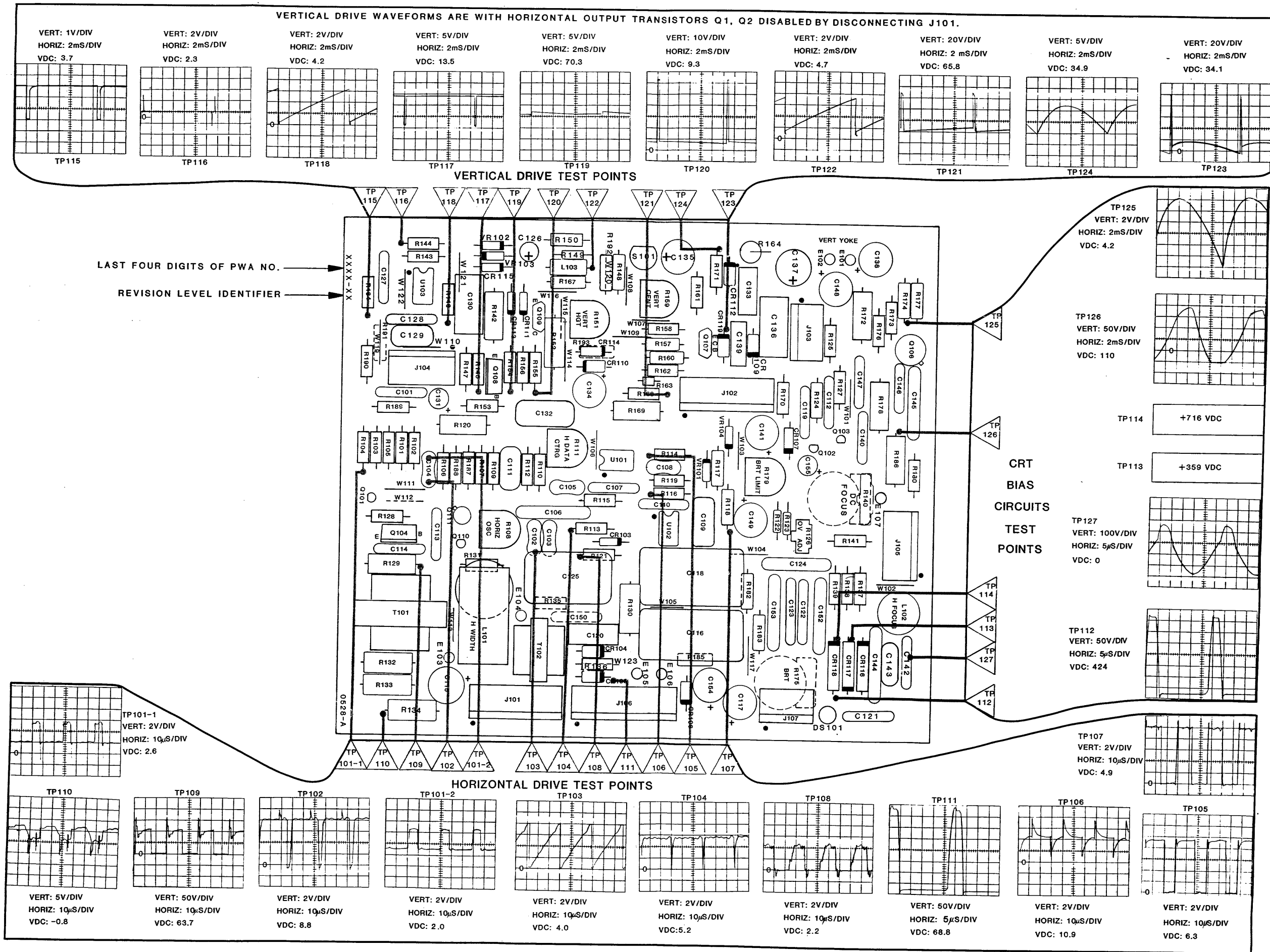
HORIZONTAL & VERTICAL TEST POINTS LOCATION, FIGURE 4-2

5620
Ball Monitor
2 of 6
(wide)
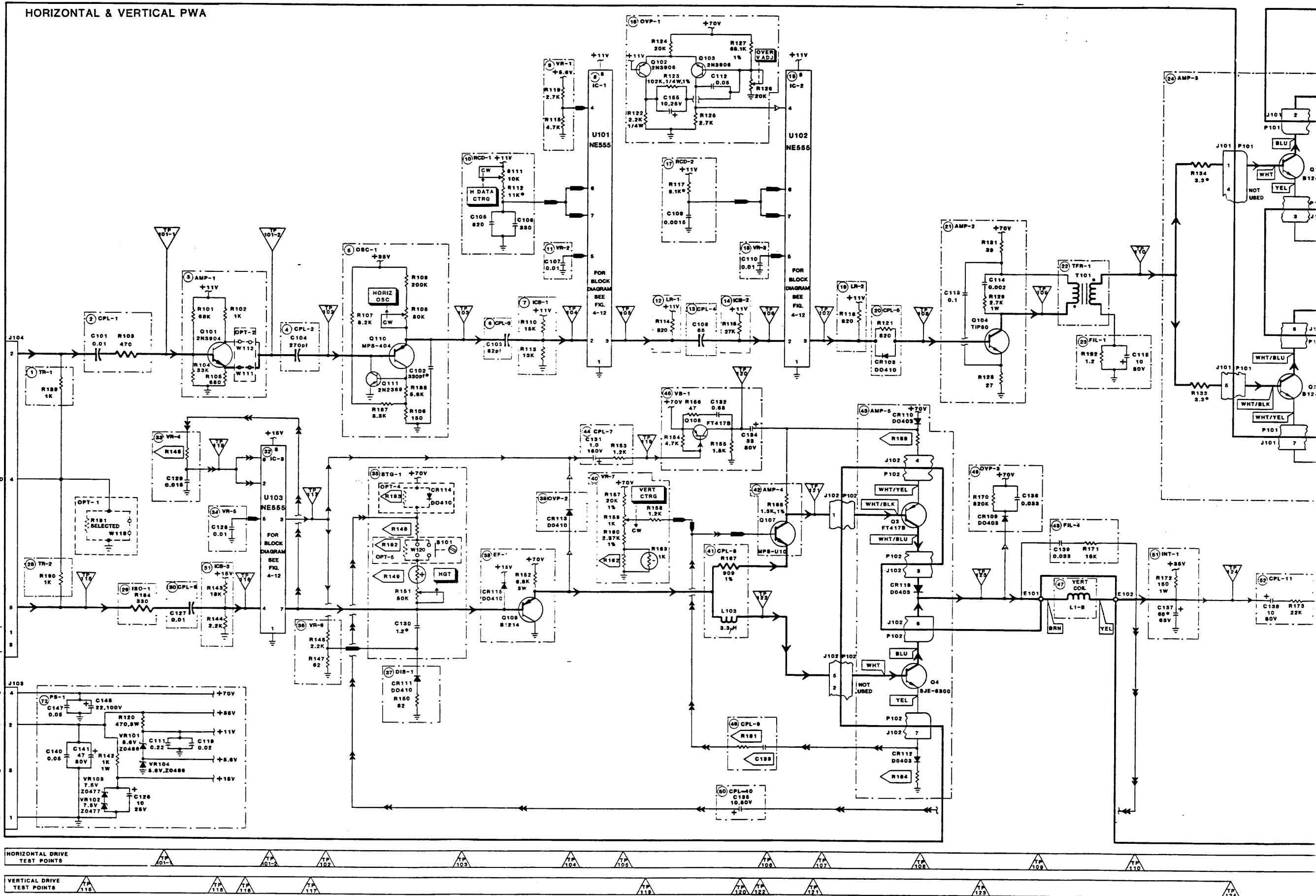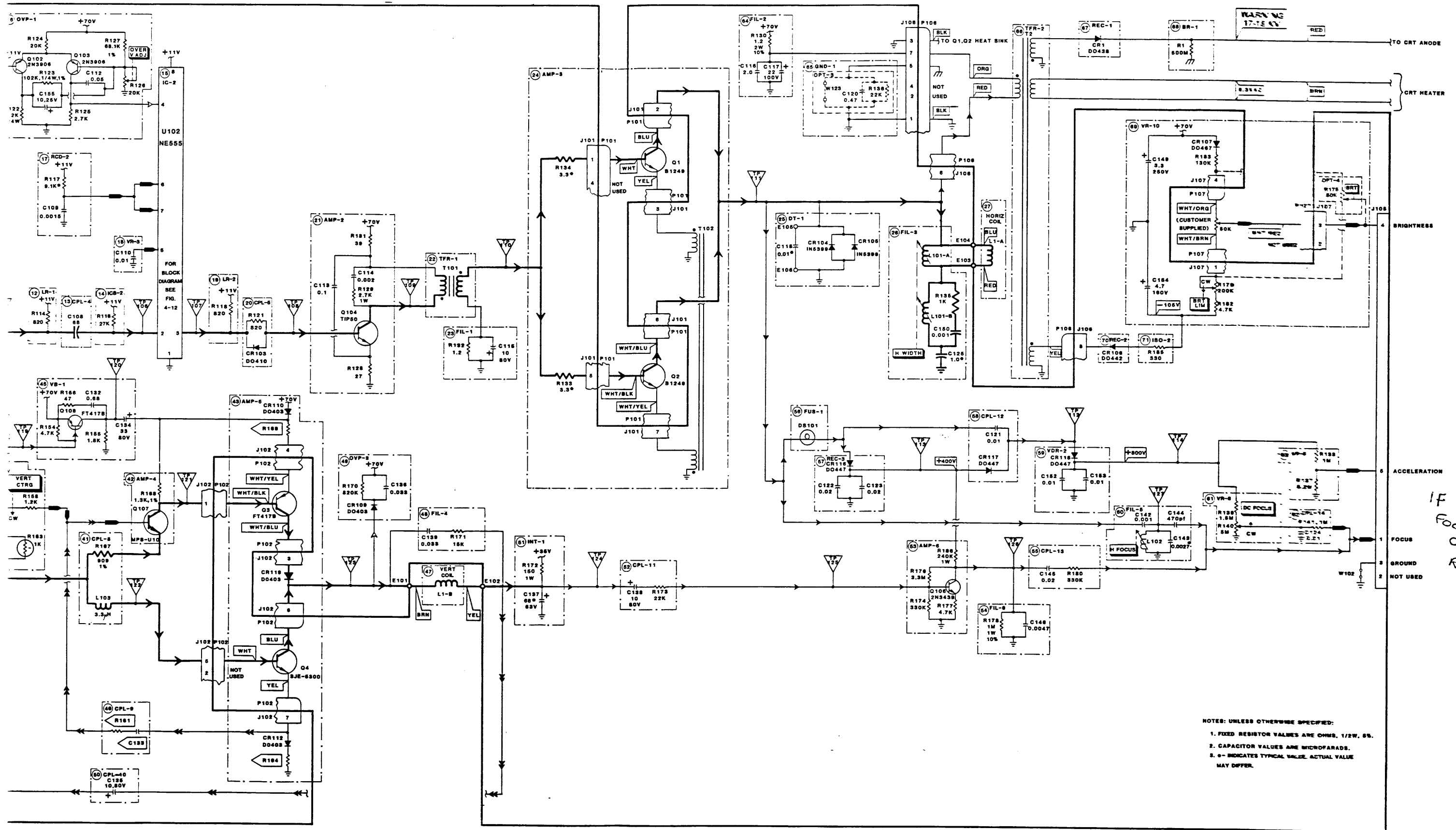
HORIZONTAL & VERTICAL FUNCTIONAL BLOCKED SCHEMATIC

FIGURE 4-3

NOTES: UNLESS OTHERWISE SPECIFIED:

1. FIXED RESISTOR VALUES ARE OHMS, 1/2W, 5%.
2. CAPACITOR VALUES ARE MICROFARADS.
3. * INDICATES TYPICAL VALUE, ACTUAL VALUE MAY DIFFER.

LAST FOUR DIGITS OF PWA NO.— —REVISION LEVEL IDENTIFIER

Cold solder or open connections often occur on Q201, Q205, and Q206. Resolder to fix video.

XXXX-XX

TP206
VERT: 10V/DIV
HORIZ: 5mS/DIV

TP205
VERT: 10V/DIV
HORIZ: 5mS/DIV

TP204
VERT: 2V/DIV
HORIZ: 5mS/DIV

TP207
VERT: 10V/DIV
HORIZ: 5mS/DIV

TP208
VERT: 100V/DIV
HORIZ: 5mS/DIV

TP201
VERT: 0.5V/DIV
HORIZ: 5mS/DIV

TP203
VERT: 1V/DIV
HORIZ: 5mS/DIV

TP202
VERT: 1V/DIV
HORIZ: 5mS/DIV
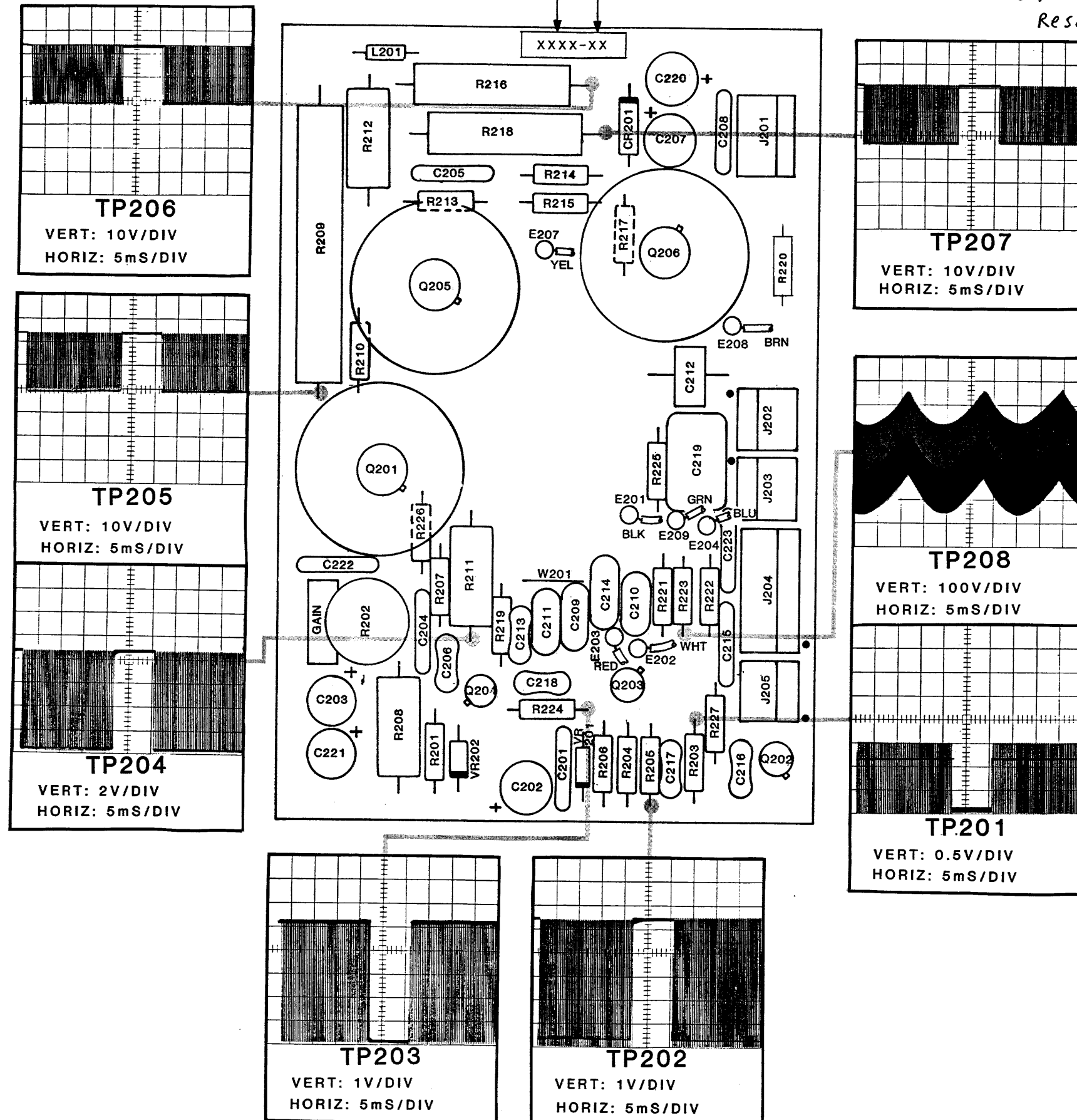
TTL VIDEO AMPLIFIER TEST POINTS LOCATION, FIGURE 4-4

TTL VIDEO AMPLIFIER PWA

NOTES: UNLESS OTHERWISE SPECIFIED
1. FIXED RESISTOR VALUES ARE OHMS ,1/2W,5%
2. CAPACITOR VALUES ARE MICROFARADS.
3. Q201,Q205,Q206 REQUIRE HEAT SINKS.
4. ARC GAP TO ALL CRT SOCKET PINS.

TTL VIDEO AMPLIFIER FUNCTIONAL BLOCKED SCHEI
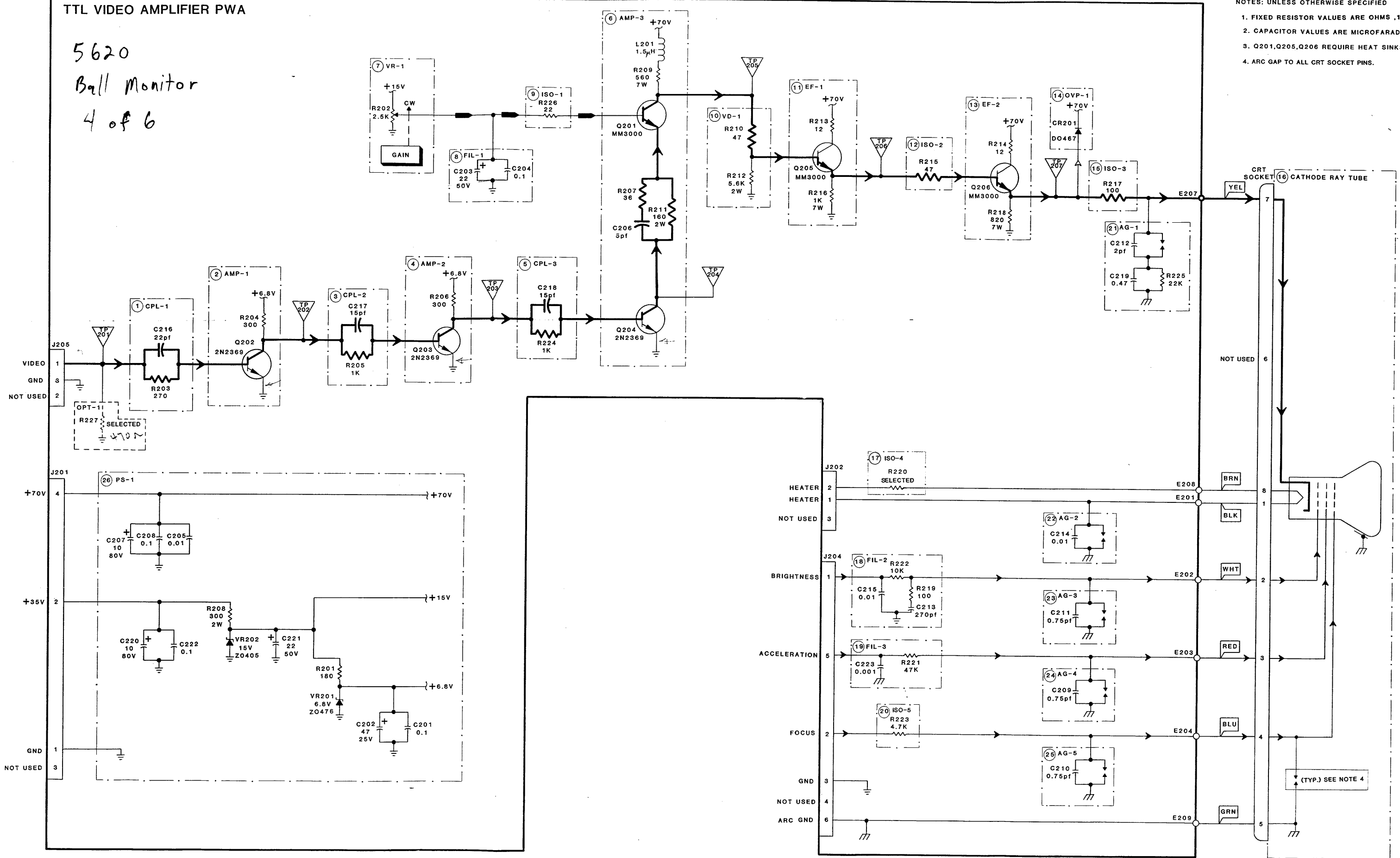
FIGURE 4-5

TTL VIDEO AMP TEST POINTS

TP 201 TP 202 TP 203 TP 204 TP 205 TP 206 TP 207

J205
VIDEO 1
GND 3
NOT USED 2

OPT-1 R227 SELECTED

① CPL-1
C216 22pf
Q202 2N2369
R203 270

② AMP-1 +6.8V
R204 300
Q203 2N2369

③ CPL-2
C217 15pf
R205 1K

④ AMP-2 +6.8V
R206 300
Q204 2N2369

⑤ CPL-3
C218 15pf
R224 1K

⑥ AMP-3 +70V
L201 1.5μH
R209 560 7W
Q201 MM3000
R207 36
R211 160 2W
C206 5pf

⑦ VR-1 +15V
R202 2.5K CW
GAIN

⑧ FIL-1
C203 22 50V
C204 0.1

⑨ ISO-1
R226 22

⑩ VD-1
R210 47
R212 5.6K 2W
R216 1K 7W

⑪ EF-1 +70V
R213 12
Q205 MM3000

⑫ ISO-2
R215 47

⑬ EF-2 +70V
R214 12
Q206 MM3000
R218 820 7W

⑭ OVP-1 +70V
CR201 DO467

⑮ ISO-3
R217 100

㉑ AG-1
C212 2pf
C219 0.47
R225 22K

E207 YEL 7

CRT SOCKET ⑯ CATHODE RAY TUBE

NOT USED 6

J201
+70V 4
+35V 2
GND 1
NOT USED 3

㉖ PS-1
+70V
C207 10 80V
C208 0.1
C205 0.01
C220 10 80V
C222 0.1
R208 300 2W
VR202 15V Z0405
C221 22 50V
+15V
R201 180
VR201 6.8V Z0476
+6.8V
C202 47 25V
C201 0.1

J202
HEATER 2
HEATER 1
NOT USED 3

⑰ ISO-4
R220 SELECTED

E208 BRN 8
E201 BLK 1

⑳ AG-2
C214 0.01

J204
BRIGHTNESS 1
ACCELERATION 5
FOCUS 2
GND 3
NOT USED 4
ARC GND 6

⑱ FIL-2
R222 10K
C215 0.01
R219 100
C213 270pf

⑲ FIL-3
C223 0.001
R221 47K

⑳ ISO-5
R223 4.7K

㉒ AG-2
C214 0.01
E202 WHT 2

㉓ AG-3
C211 0.75pf
E203 RED 3

㉔ AG-4
C209 0.75pf
E204 BLU 4

㉕ AG-5
C210 0.75pf
E209 GRN 5

(TYP.) SEE NOTE 4

TP302 +35V

TP301 +70V

LAST FOUR DIGITS OF PWA NO.

REVISION LEVEL IDENTIFIER

POWER SUPPLY TEST POINTS LOCATION, FIGURE 4-6

5620
Ball Monitor
6 of 6
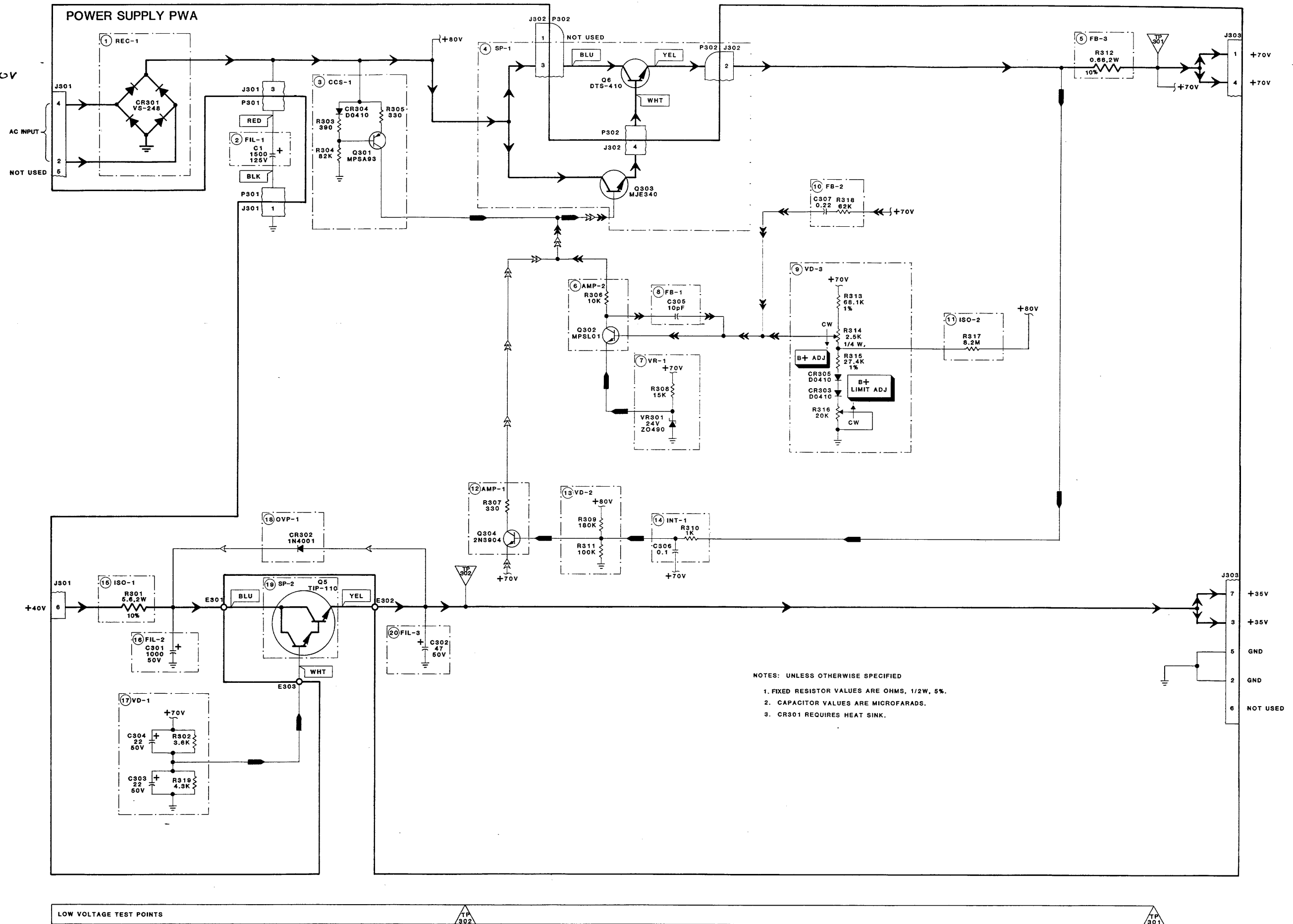
POWER SUPPLY FUNCTIONAL BLOCKED SCHEMATIC, FIGURE 4-7

5620
Power supply

CODE	ZONE	CODE	ZONE	CODE	ZONE	CODE	ZONE	CODE	ZONE	CODE	ZONE	CODE	ZONE	CODE	ZONE	CODE	ZONE	CODE	ZONE	CODE	ZONE	CODE	ZONE	CODE	ZONE	CODE	ZONE	CODE	ZONE	CODE	ZONE
B01	E7	C15	B3	C21	D2	C28	D2	C5	D6	D11	C3	D4	D4	IC1	D3	L6	D2	Q7	A2	R15	B3	R21	B2	R28	C2	R34	C2	R41	C1	SCR1	C2
C1	D8	C16	D3	C22	D3	C29	C2	C6	D6	D12	D3	D5	B3	IC2	C3	Q1	D5	R1	E8	R16	D3	R22	B2	R29	C2	R35	C1	R42	D8	T1	E8
C10	D5	C17	D3	C23	C3	C3	D7	C7	D6	D13	D3	D6	B3	L1	E6	Q3	B3	R10	E4	R17	D3	R23	B2	R3	D6	R36	B1	R5	D6	T2	D5
C11	D4	C18	D3	C24	B2	C31	D7	C8	D6	D14	C3	D7	B3	L2	C6	Q4	C2	R11	D5	R18	B3	R24	A2	R30	B2	R37	B1	R6	D5	T3	D4
C12	D4	C19	D3	C25	B2	C32	C2	C9	D6	D15	C2	D8	E3	L3	D5	Q5	C2	R12	D4	R19	A3	R25	C3	R31	B1	R38	B1	R7	D5	VDR1	D8
C13	D4	C2	D7	C26	C2	C33	D7	D1	D5	D2	D3	D9	D3	L4	B3	Q6	B2	R13	D4	R2	D6	R26	C2	R32	B2	R4	D6	R8	E5	Z1	D2
C14	B4	C20	D3	C27	D2	C4	D7	D10	D5	D3	D4	F1	E8	L5	E2	Q6	C1	R14	B3	R20	B3	R27	D2	R33	C2	R40	D1	R9	D5		

* R36, R37, R38, ARE +5V OUTPUT ADJUST RESISTORS.

NOTE: THIS DRAWING WAS PREPARED BY COMPUTER. DO NOT UPDATE MANUALLY.

6	ADD R42	IVAN	WILLIAM	12JUN89	891066	
5	REVISE DRAWING	GONG	FUN	16.1.85	E14317	
ISSUE	REVISIONS	APPD	CHK	DATE	ECN	

UNLESS OTHERWISE SPECIFIED
ALL DIMENSIONS ARE IN MM
TOLERANCES:
WHOLE NO ± ANGLE ±
DECIMAL
.x ±
.xx ±

DO NOT SCALE DRAWING

	DATE	
DRN Y.F.CHAN	16.JAN.85	
CHK	16.JAN.85	
FUN	16.JAN.85	
APPD P.T.B		
GONG	16.JAN.85	

TITLE
CIRCUIT DIAGRAM

FIRST USED ON AC9262
AC9231 AC9232 AC9252

PART NO

MATERIAL

FINISH

ASTEC
HONG KONG

SH 1 OF 1 | A2

RE-2730   C I R C U I T   C O D E   L I S T I N G   B Y   M O D E L   DATE: 06/05/85
                                               TIME: 13:24:39
COMPANY: ACL   (INDENTED BILL)   PAGE: 1

Handwritten: *5620 Power Supply* — *Astec AC9252*

0123456789	ITEM NUMBER	DESCRIPTION	UM	CIRCUIT CODES
1	AC9252	POWER SUPPLY COMPLETE	PC	F1
1	084-0620000-0217	FUSE 2.5A 250V 3AG	PC	
1	851-1030892S-0000	PCB ASSY	PC	
2	055-1030821ZS-0111	CAP-C .010 +-20% 1KV 250	PC	C12 C13
2	055-1030212S-0111	CAP-C .010+80-20%100V/250	PC	C10
2	055-2220001-0189	CAP-C 2200P +-20% 400VAC	PC	C3 C4
2	055-4767728-0111	CAP-C 470P +-20% 3KV 250P	PC	C11
2	057-1013610-0111	CAP-E 56P +-10% 50V SL	PC	C16
2	057-1013010-0192	CAP-E 100U +100-10% 25V	PC	C22
2	057-1012020-0192	CAP-E 100U +50-10% 25V	PC	C31 C32
2	057-1012060-0192	CAP-E 100U +100-10% 16V	PC	C23
2	057-1012040-0192	CAP-E 1000F +-20% 250V	PC	C6
2	057-1022020-0192	CAP-E 1000U +100-10% 10V	PC	C18 C19 C20 C21
2	057-1022040-0192	CAP-E 1000U +50-10% 25V	PC	C26 C27
2	057-2212008C-0192	CAP-E 220U +50-10% 10V	PC	C9
2	058-1049029C-0192	CAP-E 47U +10C-10% 250V	PC	C7
2	058-1049029D-0220	CAP-MP 0.1UF +-10% 100V	PC	C33
2	058-2240300-0220	CAP-P .022UF +-20% 100V	PC	C25
2	068-1040010-0220	CAP-MPR .01U+-20% 250VAC	PC	C1 C24
2	068-1040010-0220	CAP-MPH .1U +-20% 250VAC	PC	C2 C14
2	075-1049010-0165	CAP-C MTY 1U0NF +50-20%	PC	C28 C29
2	146-6020050C-0258	WAFER 12 CCT	PC	SK2
2	146-0020063C-0258	WAFER 3CCT	PC	SK1
2	209-1020020-0148	TRS-NPN 2SC1358	PC	Q2
2	209-1170046D-0120	TRS-NPN 2SD467	PC	Q1 Q5 Q6
2	211-1170035D-0120	TRS-PNP 2SB561	PC	Q3 Q4
2	211-1080010D-0176	REGULATOR 431	PC	Q7
2	212-1070210-0158	DIODE-SI 1N4616	PC	D5 D6 D7
2	222-5608602-0148	DIODE-Z 5.6V +-5% 400MA	PC	Z1
2	226-1010040-0118	RECT KGP158	PC	D10 D11 D3
2	226-1040063-0118	RECT KGP10J	PC	D2
2	226-1040070-0118	RECT KGP10B	PC	D1
2	226-1040080-0118	RECT 1N4001GP	PC	D12 D13 D14 D15
2	226-1040010C-0118	RECT KGP10M	PC	D4
2	226-3050010-0118	BRIDGE RECT K8P10	PC	DB1
2	240-1000060022-0152	RES-CF 10R +-5% 1/4W	PC	R11 R16 R17
2	240-1020022-0152	RES-CF 1K +-5% 1/4W	PC	R25
2	240-1030022-0152	RES-CF 10K +-5% 1/4W	PC	R26
2	240-1040022-0152	RES-CF 100K +-5% 1/4W	PC	R31 R32
2	240-1200022-0152	RES-CF 12R +-5% 1/4W	PC	R27
2	240-1220022-0152	RES-CF 1.2K +-5% 1/4W	PC	R35
2	240-1230022-0152	RES-CF 12K +-5% 1/4W	PC	R23
2	240-1830022-0152	RES-CF 18K +-5% 1/4W	PC	R29
2	240-2710033-0152	RES-CF 270R +-5% 1/2W	PC	R15
2	240-3310022-0152	RES-CF 330R +-5% 1/4W	PC	R19
2	240-3310603-0152	RES-CF 330R +-5% 1/2W	PC	R18
2	240-3960022-0152	RES-CF 39R +-5% 1/4W	PC	R14
2	240-4710022-0152	RES-CF 470R +-5% 1/4W	PC	R7 R24
2	240-4720022-0152	RES-CF 4.7K +-5% 1/4W	PC	R30

RE-2730   C I R C U I T   C O D E   L I S T I N G   B Y   M O D E L   DATE: 06/05/85
                                               TIME: 13:25:33
COMPANY: ACL   (INDENTED BILL)   PAGE: 2

0123456789	ITEM NUMBER	DESCRIPTION	UM	CIRCUIT CODES
2	240-4730022-0152	RES-CF 47K +-5% 1/4W	PC	R34
2	240-5600022-0152	RES-CF 56R +-5% 1/4W	PC	R21 R22
2	240-5620022-0152	RES-CF 5.6K +-5% 1/4W	PC	R33
2	240-5630022-0152	RES-CF 56K +-5% 1/4W	PC	R37
2	240-5690022-0152	RES-CF 5.6R +-5% 1/4W	PC	R12 R6 R9
2	240-8210022-0152	RES-CF 820R +-5% 1/4W	PC	R5
2	240-8290022-0152	RES-CF 8.2R +-5% 1/4W	PC	R20
2	245-2220022-0152	RES-SMF 2.2K +-5% 1/4W	PC	R28
2	247-0470054-0189	RES-MF .47K +-5% 1W	PC	R13
2	247-1000054-0189	RES-MF 1R +-5% 1W	PC	R10
2	247-2701022-0189	RES-MF 2.7K +-1% 1/4W	PC	R36 R38
2	248-1040005-0189	RES-MOF 100K +-5% 1W	PC	R2 R3
2	248-1210005-0189	RES-MOF 120R +-5% 1W	PC	R8
2	248-3306063-0189	RES-MOF 33K +-5% 2W	PC	R4
2	256-3010007D-0557	VDR 3CGVAC VZA300	PC	VDR1
2	328-4097001S-0152	THMTR 4R +-20%	PC	L4
2	328-0010010-0124	CHOKE 1.5MH	PC	L3
2	852-1010030-0124	BASE CHOKE 2.2UH	PC	L6
2	852-1010370-0353	FILTER CHOKE COIL ASSY	PC	T3
2	852-1020120D-0000	PWR TRF ASSY	PC	T2
2	852-1020210-1075	CONTROL TRF ASSY (J/V)	PC	L5
2	852-2010010-0353	CHOKE COIL ASSY	PC	L1 L2
2	852-2010100-1343	TORUID ASSY	PC	T1
2	852-2020120-0522	COM MODE TRF ASSY	PC	
3	853-0020125D-0000	RECT/HTSK ASSY	PC	IC1
3	211-1030020C-012C	REGU HA178M12P	PC	IC2
3	211-1030060-0120	REGU HA178M05P	PC	IC2
3	226-1130060-0164	RECT-SCR S10SC3M	PC	D8 D9
2	227-1300C10-0196	SCR C122U	PC	SCR1

END OF REPORT

DRAWING NO.	SHEET NO.	DESCRIPTION	ISSUE NUMBER																											
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
		SCHEMATIC DIAGRAMS																														
4896SD	ALL	410896 CIRCUIT CARD ASSEMBLY	1																													
		CIRCUIT CARD ASSEMBLY																														
410896	1	CIRCUIT CARD	1																													
		CIRCUIT DESCRIPTION																														
4896CD	ALL	410896 CIRCUIT CARD ASSEMBLY	1																													

WIRING DIAGRAM PACKAGE FOR M56 KEYBOARDS (56K224 AND 56K229)   0607WDP

TELETYPE CORPORATION   27715 R   NOTE : THE LAST COMPLETED COLUMN INDICATES THE LATEST ISSUE NUMBER OF WDP.   SHEET 1 OF 1

R & D FORM 361 (6-66)

SHEET INDEX

CONTENTS	SHEET NO.	ISSUE NO. 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	SHEET NO.
SHEET INDEX, SUPPORTING INFORMATION	A1	1	2	3	4																							A1
FS-1 KEYSWITCH AND INTERFACE LOGIC	B1	1	2	3	4																							B1
NOTES:	D1	1	2	2	2																							D1
BD-1 BLOCK DIAGRAM	H1	1	2	2	2																							H1

SUPPORTING INFORMATION

CATEGORY	NO.
KEYSWITCH AND INTERFACE LOGIC CIRCUIT DESCRIPTION	4896CD
CIRCUIT CARD ASSEMBLY DRAWING	410896 410967
LOGIC SYMBOLS, TRUTH TABLES AND GENERAL NOTES	9100WD

USE OF SHEET INDEX

WHEN CHANGES ARE MADE IN THIS DRAWING:

1. ONLY CHANGED SHEETS WILL BE REISSUED. (INCLUDING SHEET 1)

2. UNCHANGED SHEETS RETAIN EXISTING ISSUE NUMBER.

THE LAST COMPLETED COLUMN ON THE SHEET INDEX INDICATES THE LATEST ISSUE PER SHEET.

SCHEMATIC DIAGRAM
FOR THE 410896,
410967 CIRCUIT CARD
ASSEMBLY

APPROVALS

PROJ. SUPV.	PROJ. DIR.	MFC. REL. COMPL.

ENGR. P.H.B. | DSGNR. P.H.B.
DRN. J.V.K. | DATE 1-20-83
R&D FILE G-18,366AA
S-NUMBER 62664S

TELETYPE CORPORATION

4896SD-A1

TC654-0579

FS-1 KEYSWITCH AND INTERFACE LOGIC

HL — KEYSWITCH POSITION NOS. (SEE FIGURE)(BELOW)

SENSE	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1
S1	92	76	56	37	13	2	26	45	65	102
S2	91	75	55	36	12	3	27	46	66	84
S3	90	74	54	35	11	4	28	47	67	103
S4	89	73	53	34	10	5	29	48	68	85
S5	104	72	52	33	9	6	30	49	69	86
S6	88	71	51	32	8	7	31	50	70	87
S7	93	77	57	38	14	24	44	64	83	105
S8	94	78	58	39	20	19	43	63	82	101
S9	95	79	59	40	15	1	25		100	106
S10	96	80	60	41	16	18	23			107
S11	97	81	61	42	21					108
S12	98		62	22	17					109
S13	99									110

DRIVE
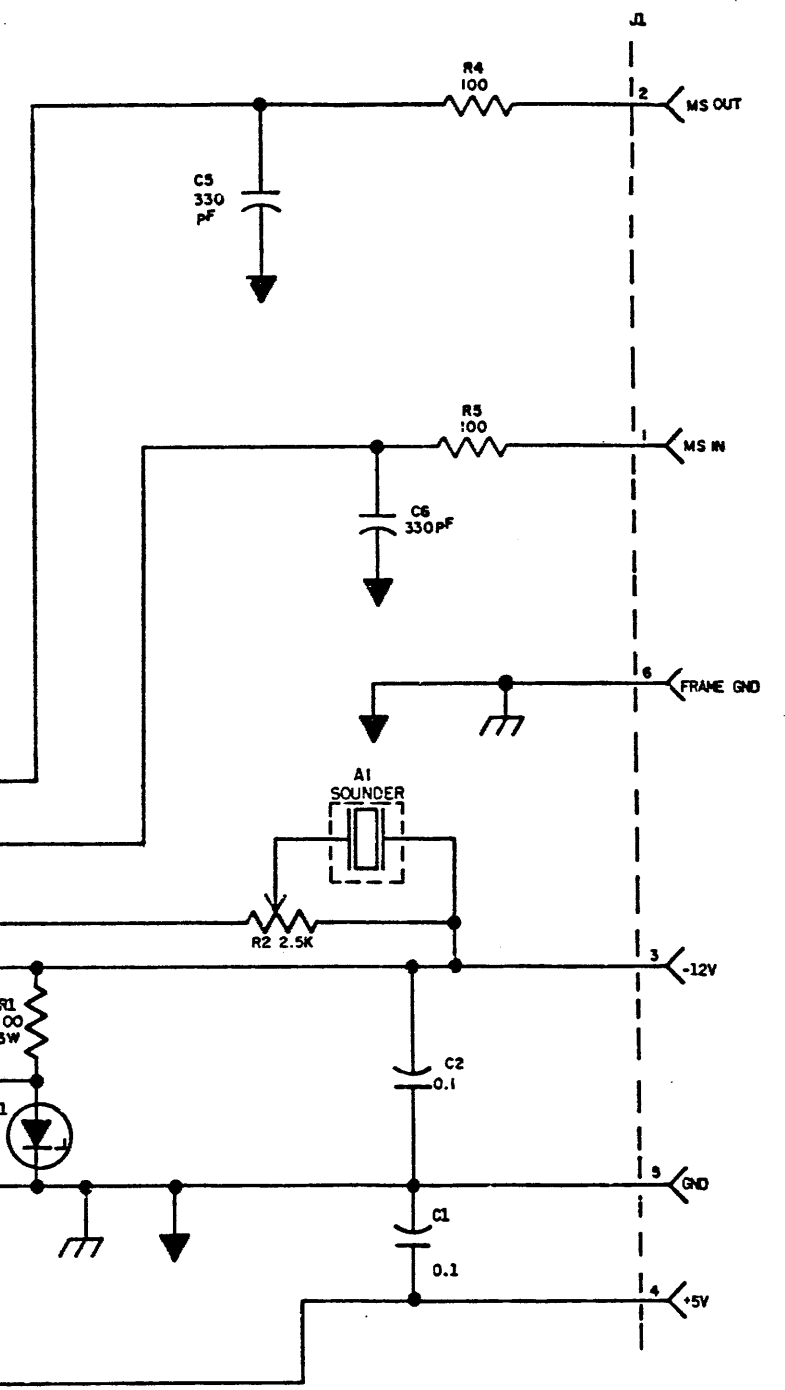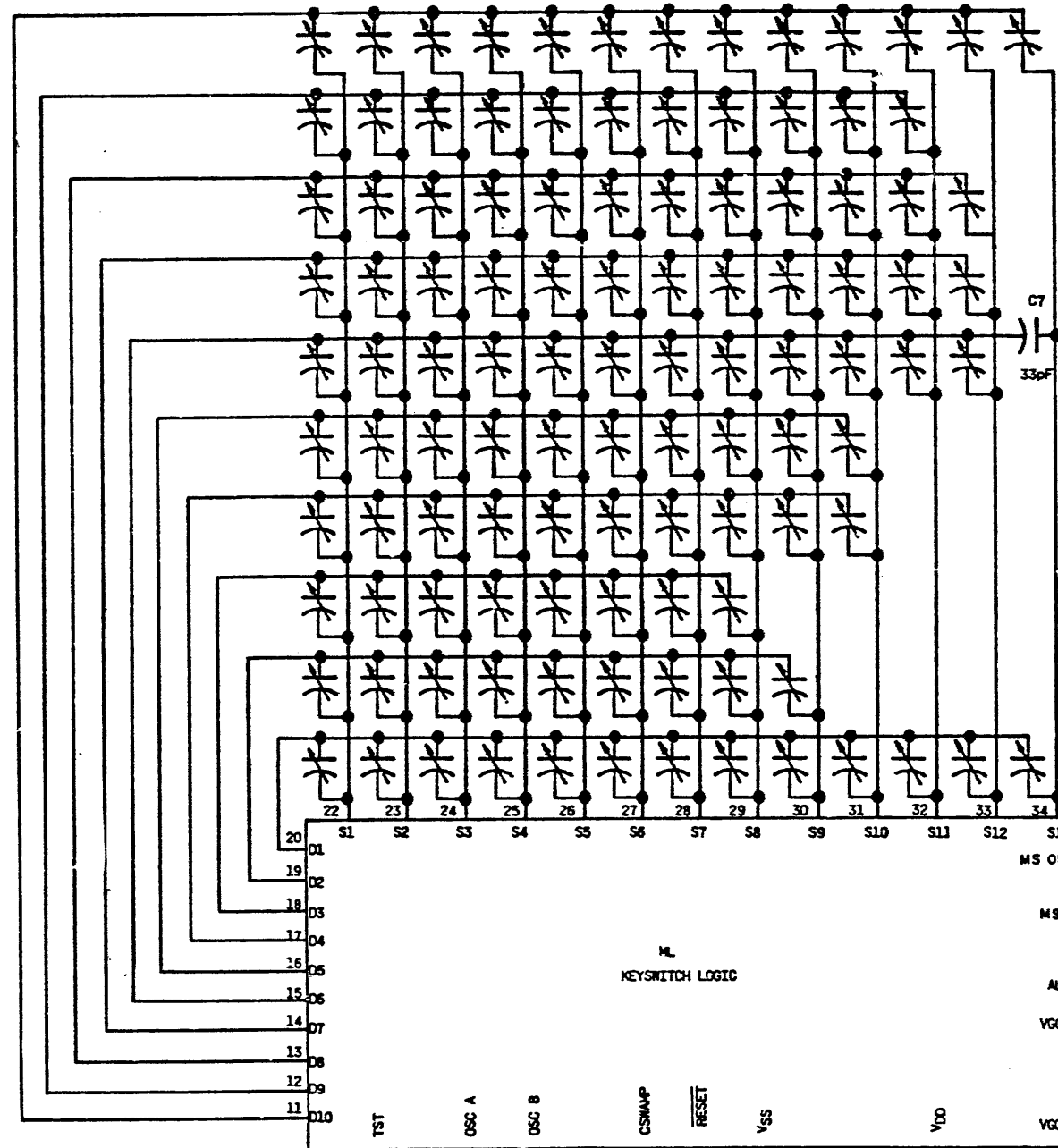
THESE KEY POSITIONS ARE FUNCTIONAL
ON THE 410967 CARD ASSEMBLY ONLY

KEYSWITCH POSITIONS

1	2		3	4	5	6	7	8	9	10	11	12	13	14		15	16	17
18	19															20	21	22
23	24		25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42
43	44		45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62
63	64		65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81
82	83		84	85	86	87	88	89	90	91	92	93	94		95	96	97	98	99
100	101		102	103				104				105	106	107	108	109	110

HL KEYSWITCH LOGIC

S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 S12 S13
22 23 24 25 26 27 28 29 30 31 32 33 34

20 D1
19 D2
18 D3
17 D4
16 D5
15 D6
14 D7
13 D8
12 D9
11 D10

21 TST
7 OSC A
8 OSC B
35 CSMAMP
37 RESET
1 VSS
10 VDD

39 MS OUT
2 MS IN
4 ALM
6 VGG2
9 VGG1

XTAL 1.8432 MHz
C3 100pF
R3 220k
C4 6.8
R1 100 3W
CR1 5.1V

C7 33pF

R4 100 — MS OUT
C5 330 pF
R5 100 — MS IN
C6 330 pF
FRAME GND

A1 SOUNDER
R2 2.5K
-12V
C2 0.1
GND
C1 0.1
+5V

J1
2
1
6
4
3
9
4

TC640-0878

O
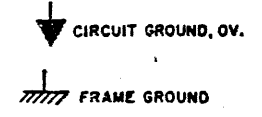
CIRCUIT NOTES

101. SUPPLY VOLTAGES:

THE FOLLOWING VOLTAGES ARE MEASURED WITH RESPECT
TO V_{DD}

+5V. ————————— V_{SS}

————————— V_{DD}

-12V ————————— V_{GG2}

102. SIGNAL VOLTAGES:

INPUT
MS IN ——— 1

410896
410967

2 OUTPUT
MS OUT

3   5   4

-12V   OV
GND.   +5V

ISSUE
1
2
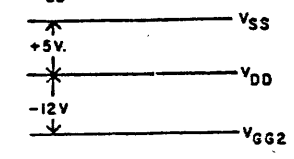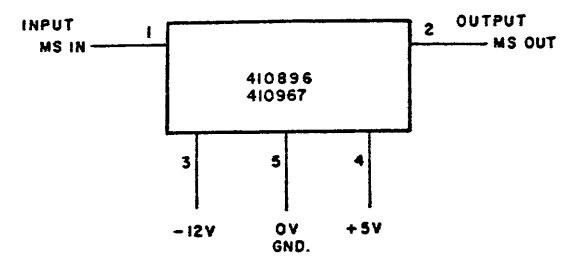
SCHEMATIC
DIAGRAM FOR THE
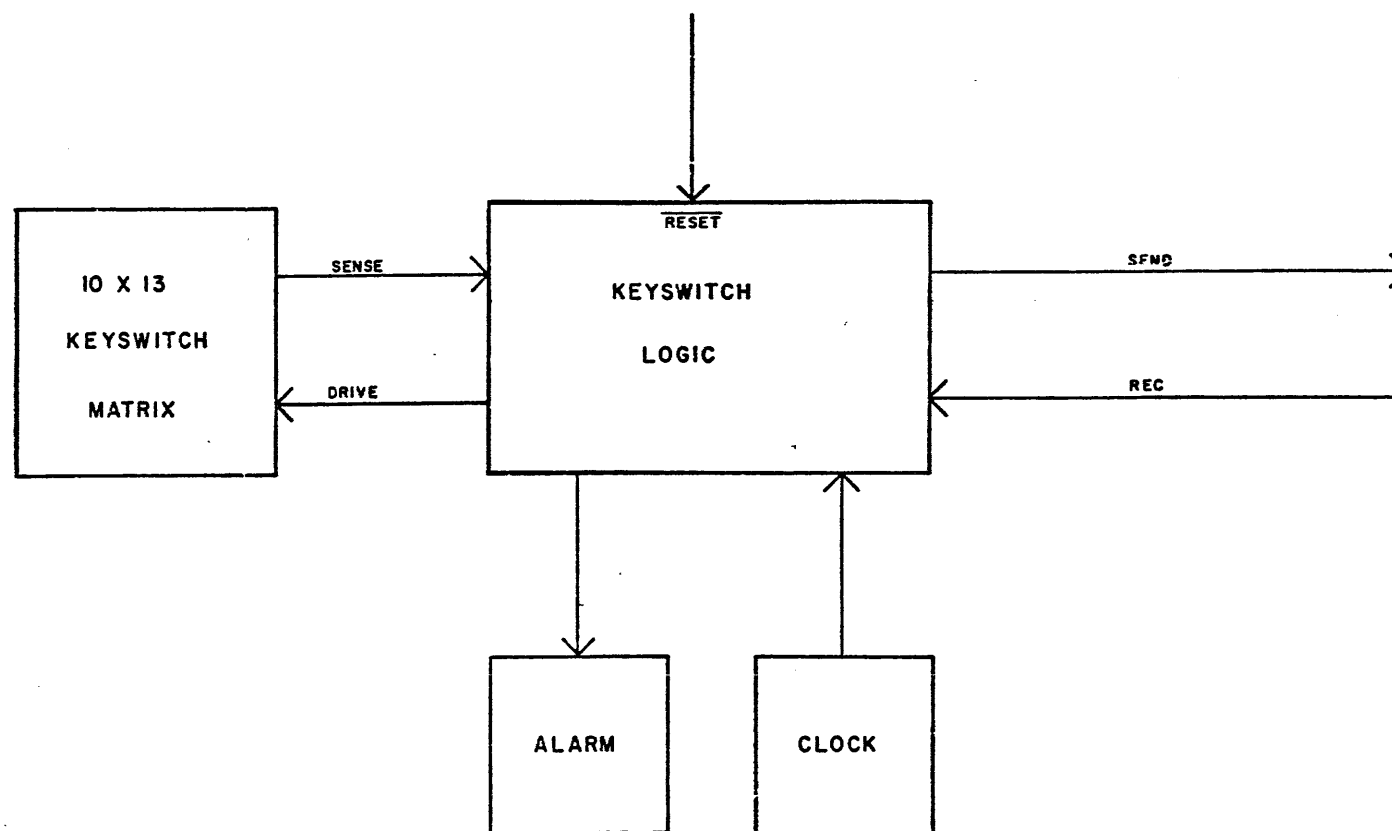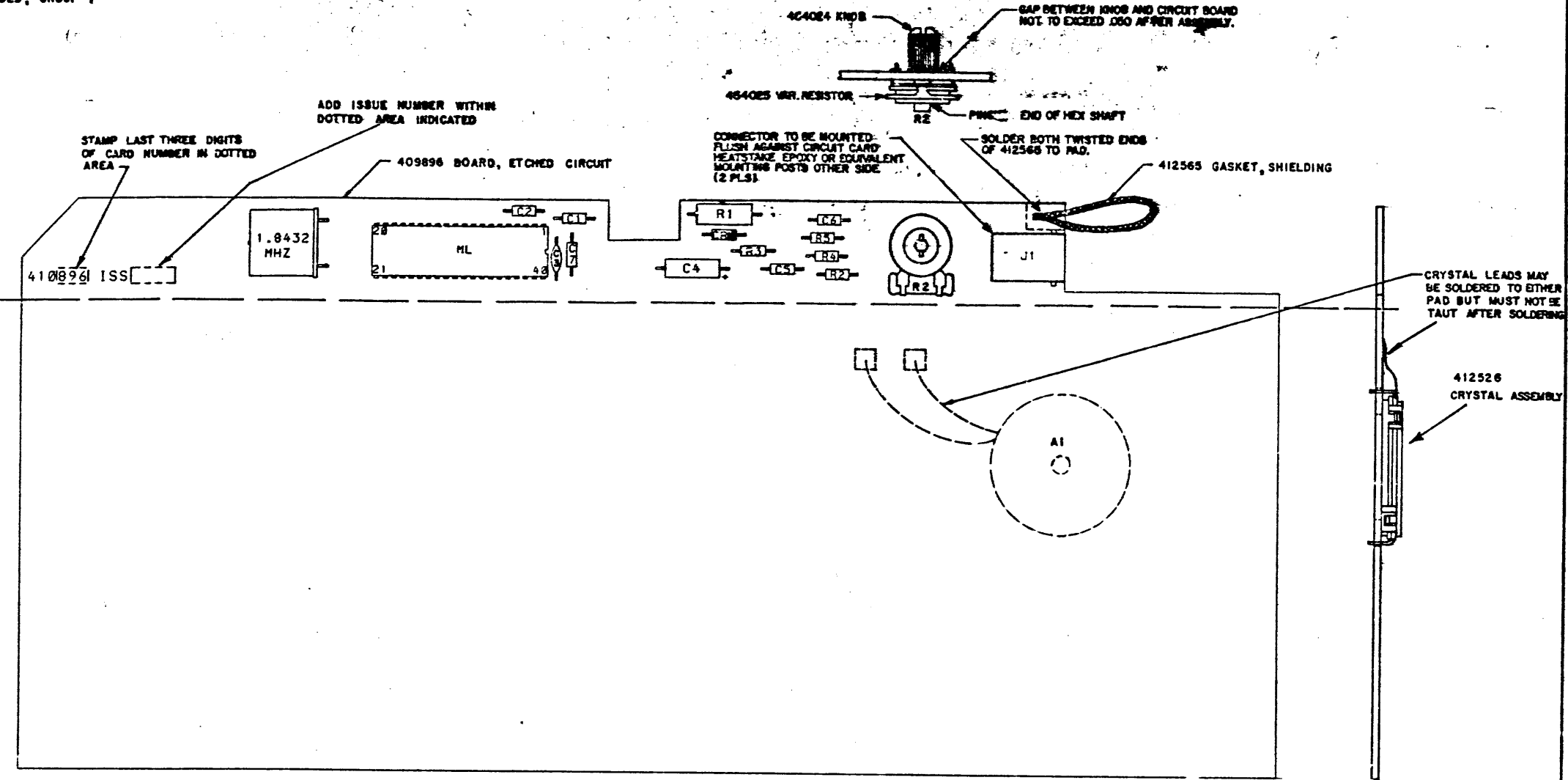410896, 410967
CIRCUIT CARD
ASSEMBLY

TELETYPE CORPORATION
SKOKIE, ILLINOIS

4896SD-DI

TC640-0781

BD-1 BLOCK DIAGRAM

```
                                    │
                                    ▼
  ┌──────────────┐              ┌─────RESET─────┐
  │              │    SENSE     │               │         SEND
  │   10 X 13    │─────────────▶│   KEYSWITCH   │──────────────────▶
  │              │              │               │
  │  KEYSWITCH   │              │    LOGIC      │
  │              │    DRIVE     │               │         REC
  │   MATRIX     │◀─────────────│               │◀──────────────────
  └──────────────┘              └───────┬───┬───┘
                                        │   ▲
                                        ▼   │
                                  ┌───────┐ ┌───────┐
                                  │       │ │       │
                                  │ ALARM │ │ CLOCK │
                                  │       │ │       │
                                  └───────┘ └───────┘
```

ISSUE
1
2

TC640-0781

NOTE: MANUFACTURE PER MR2001 AND MR2029, GROUP I

GAP BETWEEN KNOB AND CIRCUIT BOARD NOT TO EXCEED .050 AFTER ASSEMBLY.

464024 KNOB

464025 VAR. RESISTOR
R2

PIN— END OF HEX SHAFT

SOLDER BOTH TWISTED ENDS OF 412565 TO PAD.

412565 GASKET, SHIELDING

STAMP LAST THREE DIGITS OF CARD NUMBER IN DOTTED AREA

ADD ISSUE NUMBER WITHIN DOTTED AREA INDICATED

409896 BOARD, ETCHED CIRCUIT

CONNECTOR TO BE MOUNTED FLUSH AGAINST CIRCUIT CARD HEATSTAKE EPOXY OR EQUIVALENT MOUNTING POSTS OTHER SIDE (2 PLS)

410896 ISS[___]

1.8432 MHZ

ML

C2 C1

R1

C4

C3

R3 R5 R9

C4 C5 R2

J1

R2

NOTE 2

CRYSTAL LEADS MAY BE SOLDERED TO EITHER PAD BUT MUST NOT BE TAUT AFTER SOLDERING

412526 CRYSTAL ASSEMBLY

A1

MANUFACTURING NOTES
1. ALL AREAS OF KEYSWITCH PADS WHICH MAKE UP KEYSWITCH CAPACITOR TO BE FREE OF FLUX.
2. COMPONENT PIN PROTRUSION THROUGH CIRCUIT BOARD ON NON-COMPONENT SIDE .045 MAXIMUM IN AREA ABOVE DASHED LINE.

CUSTOMERS NOTES:
1. CUSTOMER IDENTIFICATION ISSUE 2A, R-2 4H252 CHANGED TO R-2 454025 VARIABLE RESISTOR WITH 464024 KNOB.
2. CUSTOMER IDENTIFICATION ISSUE 3A, ML CHANGED FROM 411881 KIKEY4 (1 SEC. REPEAT DELAY) TO 416914 KDKE4P (1/2 SEC. REPEAT DELAY).

REF. DESIG	PART NO	REQ	DESCRIPTION
ML	416914		MOS, KDKE4P
C1	405324		CAPACITOR, 0.1μF
C2			SAME AS C1
C3	328792		CAPACITOR, 100pF
C4	333727		CAPACITOR, 6.8μF
C5	335800		CAPACITOR, 330pF
C6			SAME AS C5
C7	346238		CAPACITOR, 33pF
R1	147953		RESISTOR, 100 OHMS, 3W
R2	454025		RESISTOR, VAR. 2.5K
R3	411298		RESISTOR, 220K
R4	411218		RESISTOR, 100 OHM
R5			SAME AS R4
XTAL	414554		CRYSTAL 1.8432 MHz
A1	412526		CRYSTAL ASSEMBLY
CR1	328013		DIODE, ZENER 5.1V
	454024		KNOB
	409896		ETCHED CIRCUIT BOARD
J1	412525		JACK
	412565		GASKET, SHIELDING

SIMILAR TO:
TC661/65-0102

SHEET INDEX AND ISSUE CONTROL

4896CD

CIRCUIT DESCRIPTION FOR THE 410896 AND 410967 CIRCUIT CARD ASSEMBLIES

PAGE 1 OF 1

REVISIONS			SHEET NUMBER				
ISSUE	DATE	AUTH. NO.	1	2	3	4	
1	5-24-83	27756R	1	1	1	1	
2	5-24-83	27169	2	2	2	2	
3	2-27-84	27753	2	3	2	2	

SHEET ISSUE NUMBER

APPROVALS

ENG. SAH	DSGNR.	DRN.

PROJ. SUPV.	PROJ. DIR.	MFG.REL. COMPL.	DATE		S-NUMBER
		JJK	R & D FILE NO. G-18.184AA		E-NUMBER

TELETYPE CORPORATION

4896CD

TC482-0579

CIRCUIT DESCRIPTION FOR THE
410896 AND 410967 KEYBOARD CIRCUIT CARD ASSEMBLIES

SECTION I - GENERAL DESCRIPTION

1. BASIC FUNCTIONS

1.1 The 410896 and 410967 circuit card assemblies contain capacitive keyboard encoding logic and interfacing logic for the 56K224, 56K229 and 56K230 keyboards.

1.2 The keyboard functions as a serial device and obtains its power (+5V and -12V) from the associated controller.

1.3 The keyboard encoding and serial interface logic is resident in the Teletype Corporation MOS integrated circuit, ML.

1.4 Aside from the ML MOS circuit, the card assembly contains the following:

1.4.1 The serial receiver (MS IN) front end circuit consists of resistor R5 and capacitor C6. This network is a low pass filter arrangement. Its function is to reduce noise susceptibility and provide some protection from transients (such as electro-static discharge).

1.4.2 The serial driver (MS OUT) front end circuit consists of resistor R4 and capacitor C5. This network is a low pass filter arrangement. Its function is to reduce noise susceptibility and provide some transient protection.

1.4.3 Alarm output circuitry consisting of R2 variable load resistor (volume control) and A1 sounder.

1.4.4 The C3 swamp capacitor adds a fixed capacitance to the comparator input in ML and provides a reference with which to view the key capacitance.

1.4.5 The R3 resistor and C4 capacitor comprise the external reset network for the ML circuit. On power-up, when the capacitor charges up to a nominal of 2V, the ML circuit logic comes out of reset and begins its initialization procedures.

1.4.6 The C7 capacitor provides a constant capacitor load to simulate a depressed keyswitch and is scanned during self-test.

1.4.7 Drive to sense line coupling capacitors for sensing keyswitch state are in the form of a matrix array of circuit card split lands.

SECTION II - DETAILED DESCRIPTION

1. ASSOCIATED DOCUMENTS

4896 SD Schematic Drawing of the circuit card
410896 Circuit Card Assembly Drawing
410967 Circuit Card Assembly Drawing

2. THEORY OF OPERATION

2.1 Power-On Reset/Initialization:

The ML MOS circuit begins initialization on power-up after it comes out of reset. Initialization resets all internal registers and sets all keys released. The controller can also initialize the keyboard by sending the appropriate command in a serial control word.

2.2 Self-Test Sequence

The self-test mode can be entered in three ways. The controller can send the command in a serial control word; or the keyboard operator can initiate self-test by depressing specific keys on the keyboard; or on power-up after ML has initialized itself.

Self-test interrogates the presence of C7 capacitor in the keyboard matrix location, and if present, the test is good. If the test is done during power-up, the result affects the ~Ready bit in the status word to the controller. The tilde, ~, in a signal name indicates logical negation, i.e. the signal is active low. The tilde has the same meaning as a bar drawn over the name. If the test result is good the ~Ready bit is reset. If the self-test was initiated by a command (either from the controller or the keyboard), a good test rings the alarm for approximately one second. Status is sent after the self-test.

2.3 Alarm Operation

The alarm clock (approx. 3kHz) is generated within ML and is derived by dividing the input clock. The normal alarm output has a 4-level stepped decay amplitude and the full ring lasts for about 750 ms. The "chirp" alarm sounds for 16 cycles of the alarm clock at maximum level. The chirp alarm is sounded on all key depressions if the keyboard is optioned by a command from the controller.

2.4 Keyswitch Validation and Repeat Logic

Keyswitch validation is accomplished when the sense algorithm embodied in ML is satisfied for keyswitch depression and release. The keyswitch logic in ML scans the states of all the keys every 5.35 milliseconds. There are 10 drive lines (D1 through D10) and 13 scan lines (S1 through S13). The ML sends a 10V pulse on the selected drive line and senses the states of the keys on the 13 scan lines. A key must exhibit the same condition (whether depressed or released) for two consecutive scans in order to validate the keyswitch state.

2.4 Keyswitch Validation and Repeat Logic (Cont.)

The keyboard enters the repeat mode when a single sendable key is held down for one second or more. However, if a self-test command is received in the meantime, the one second timer services the self-test, since it has priority over usage of the timer.

2.5 Sending Logic and Interface

When the keyswitch has been validated as depressed, ML will determine if the code is to be sent as character or if it is to modify the code of another keyswitch (e.g. if the keyswitch is Caps. Lock, Shift or Control, which are mode changes). If it is a character code, it will be sent as the appropriate serial data word to the controller. If it is a mode change, it will be sent in the appropriate serial status word to the controller. Control and shift key changes affect character code but do not initiate a status word.

3. POWER REQUIREMENTS

The circuit card requires +5V (±10%) at 105mA max. and -12V (±10%) at 100mA.